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Industrial Electrical Engineering and Automation

Modeling and Optimization of Silicon Carbide Converters for Traction Applications

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Abstract

The objective of this thesis is to create a tool that can help estimate a low cost and efficient design of a silicon carbide converter, two solutions are presented using different modulation schemes. A method for modeling power losses and thermal behavior of a silicon carbide based three phase two level converter is presented. The semiconductor area in combination with specific component costs are identified as cost drivers. The first solution is implemented in an optimization loop that minimizes the total semiconductor area for a given operating point, the second solution is realized using more straight forward method where a large matrix of inputs is researched. The main practical purpose for this model is to be utilized as an alternative to conventional silicon based converters in a full drivetrain optimization program. The data for modeling the parameters used in the optimization is based on bare die, discrete component data sheets of silicon carbide MOSFETs and Schottky diodes from Wolfspeed. The component data is used to create functions and maps which in turn, are used to calculate the losses for any given converter size. Two different modulation schemes are implemented, one with and one without reverse conduction of the MOSFETs. The result of the model consists of total converter cost with the number and size of SiC MOSFETs and diodes for a given operating point. A magnitude validation of the currents through each semiconductor component was performed by a comparison to a LTspice model with the equivalent operating point and the pre-existing LTspice versions of the modeled components.

Keywords: Silicon Carbide, MOSFET, converter, Loss estimation, Reverse conduction, Area optimization

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TABLE I: Acronyms

Si	Silicon
SiC	Silicon Carbide
GaN	Gallium Nitride
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
IGBT	Insulated Gate Bidirectional Transistor
PEC	Power Electronic Converter
PE	Power Electronic
EV	Electrical Vehicle
PMSM	Permanent Magnet Synchronous Machine
DTOP	Drive Train Optimization Program
EMI	Electromagnetic Interference
DCB	Direct Copper Bonded
SPWM	Sinusoidal Pulse Width Modulation
MRC	Modulation Using Reverse Conduction
MFD	Modulation Using Diode for Freewheeling Exclusively
FWD	Freewheeling diode
CoD	Coefficient of Determination
WBG	Wide Band Gap

I. Introduction

The research for this thesis has been conducted at BorgWarner in cooperation with the Industrial Electrical Engineering and Automation department (IEA) and Production and Materials Engineering (IPROD) at the Faculty of Engineering, Lund University. This chapter introduces the thesis with the problem background, aim of this thesis, related work, limitations and an outline of the thesis.

A. Background

Due to climate change, the mission of reducing CO_2-emissions is more important than ever. The transition to a greener society is already on the way and green energy from solar, wind and water together with electrical vehicles are a very important part of this. What all these technologies have in common is that they need an efficient way to transform energy from one form to another. It could be inverting the direct battery current from a car to three phase AC for the electric motor, transfer DC from a solar power field to AC for the power grid or adjust the frequency of the power from a wind turbine.

Personal transportation by private vehicles is a big contributor to the still increasing CO_2-emissions, and therefore a transition to EVs is beneficial for the environment, assuming the vehicle is charged using clean energy sources [1]. The electrical vehicles of today are more expensive than their combustion engine counterparts due to higher drivetrain and energy storage costs. Reducing these costs is vital if the transition to EVs is to be successful. One way to reduce these costs is to optimize the drivetrain of the vehicles, allowing for better utilization of the energy storage unit and a more energy efficient vehicle overall.

In todays traction converters the most common semiconductor material is Silicon (Si). On the positive side, Si is cheap and easy to process, additionally Si three phase converters can reach peak efficiencies of 98 % as of today [2]. However, the automotive applications would benefit from the traction converters being able to operate at higher modulation frequencies and at higher temperatures. This would be beneficial since it would reduce motor losses, wear and reduce cooling demands [3]. This problem is difficult to solve without looking into other wide band gap (WBG) semiconductor materials such as silicon carbide (SiC) or gallium nitride (GaN).

SiC offers many of the sought after properties that are needed for improving the performance of the traction converter. Under similar conditions SiC has lower losses than Si [3] and the technology can handle higher temperatures [4]. The property of SiC being able to handle higher temperatures can e.g. lead to some fundamental positive changes in the cooling topology.

B. Objective of this thesis

The objective of this thesis is to develop a loss and thermal model for SiC based components which is used to optimize the total cost and size of a SiC based converter. Since the area of the semiconductor devices is identified as the main cost driver [5] together with the specific component cost, this is used as the base for the optimization.

Goals:

- Create a generic, flexible and relatively fast tool to optimize the required semiconductor cost and area for a given application.
- Make the program so that only small changes are needed if the application is changed.
- Model the parameters for SiC components as accurate as possible using data available on the market today.

C. Methodology

SiC components, such as MOSFETs and Schottky diodes are modeled using data extracted from datasheets. Using these component models, the losses of the converter can be calculated for a wide range of input specifications. For a given component size the losses are calculated at the specified operating point. Followed, a thermal model is used to estimate the junction temperature, if the result differs from the target, the semiconductor area is adjusted and the whole process repeated. When this is completed the components are optimized to a minimal area for the maximum allowed temperature. This area is then used together with specific cost per area for the component, diode or MOSFET, to estimate the total converter cost.

D. Model applications

The main application of the developed tool, to optimize the size of the SiC semiconductors in power electronic converters, is to serve as an alternative to the conventional Si converter in a drivetrain optimization program, DTOP, developed by Gabriel Domingues and Pontus Fyhr at LTH. The previously developed DTOP that scales several parts in the drivetrain of an electrical vehicle [6], can be expanded by adding a loss model for a SiC MOSFET power electronic converter (PEC). The main outline of their PEC loss model is used to structure the loss model of the SiC PEC, so that it is integrated into the DTOP. Fig. 1 shows where the loss model would be used in the DTOP.

Since the model structure is made so that the optimizing is done on MOSFET- diode pairs, this means that the model quite easily may be expanded and altered to fit other PEC applications. The easiest alteration would be other applications where converters are used such as solar power to grid connections but it could also be changed to fit other power electronic applications if the inputs are matched with the new application. For applications where smaller currents are used compared to the mentioned above it is recommended to update the model since the parameters in this model are generally more accurate for larger currents.

E. Related Work

Gabriel Domingues and Pontus Fyhr's DTOP for electrical vehicles [6], provides the main application for the models developed in this thesis. The DTOP model allows the user to choose from different powertrain concepts, for example single speed transmission or two speed. A wide range of EMs is generated after selecting a PMSM design. The number of turns, axial length and overloading capabilities are optimized together with the correct sizing of the PEC and gearbox in order to meet the requirements of the application. In the DTOP, a loss model of a Si IGBT PEC is created to be able to size the PEC accordingly.
T. Friedli and J. W. Kolars' work [7] describes an area estimation algorithm with which can be used to optimize the chip area of both the transistor and the diode in a 3-phase converter, which is used in the DTOP. The optimization approach taken in this thesis is similar, based on the assumption that the correlation between chip size and total converter cost is strong [5].

F. Limitations

The differently sized transistors and diodes used to create the loss model, needed to be the same transistor technology for the loss model to be representative of a SiC technology. The best way to achieve this was to gather all data from the same company. Since the loss model is made from data from only one company, the final model is not applicable to different SiC transistor families, without generating new data.

Blanking time is left out of the loss model for brevity. It is however implemented in both the simulations used for validation which causes some error, but the effects are considered negligible.

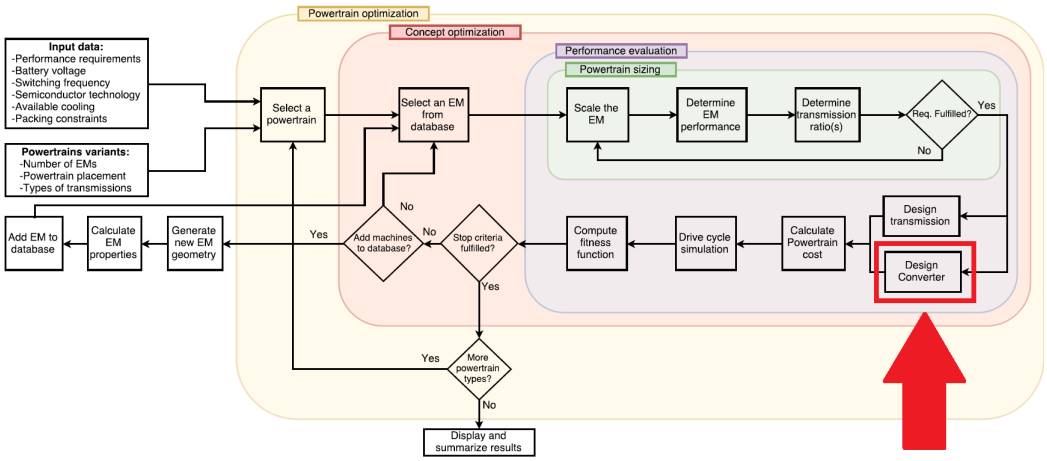

Fig. 1: In this complete drivetrain optimization loop [6], the work of this thesis is focused on the block labeled Design Converter within the Performance evaluation section [8].

Using the modulation scheme with no reverse conduction, a portion of the freewheeling current can go through the internal diode of the MOSFET, provided that the current is large enough. This is left out of the model since currents this large results in unreasonably high temperatures.

One of the main advantages of using SiC in the traction converter is the possibility to increase the switching frequency, since this can reduce motor losses by reducing the current ripple. The motor losses that come from current ripple are however not included in the DTOP. This means that these effects of increased switching frequency can not be seen in the results of this thesis.

The possibly increased EMI caused by increased switching frequency is not discussed in this thesis but should be recognized.

The higher operating temperature of SiC compared to Si opens up the alternative of sharing cooling liquid with other power components in the drivetrain. With the loss model using a static thermal model, such a change is not possible.

Both modulation schemes implemented in this model are sinusoidal modulation schemes, with the difference that one of them is not enabling the reverse conduction capabilities of the MOSFET. The model is only valid for sinusoidal modulation with a modulation index no larger than one.

In the DTOP a rigorous cost modeling is performed for the complete drivetrain of an electric vehicle. The main cost driver in the cost modeling of the converter, is the semiconductor chip area, as previously mentioned. In this work this is the only parameter to be considered, since the rest is handled in the DTOP.

With the assumption that cost is linearly dependent on chip area [5], the cost per square millimeter can be calculated from only one cost quote. This was all that was available at the time of writing this thesis. The quote was however from a different family of SiC bare dies than the ones used for the loss modeling. The performance of the chip from this quote is better than the ones used for the loss modeling and therefore

an assumption that the price is not underestimated is made. With only one quote, and with it being from a newer family of SiCs, uncertainty is introduced. The cost parameter is however handled as an input parameter and can also be set as a relative difference between the cost of the MOSFET and the diode.

G. Outline of thesis

Theory: The needed underlying theory for this thesis is presented and explained in this chapter. The operation of a single switch and a complete three phase converter is presented, along with gate driver operation, current split, loss calculation and the thermal modeling.

Method: The approach and methods used in the thesis are explained and the work flow from the initial literature study to the validation phase is presented.

Modeling and Optimization: The design of the loss model, and how the theory is applied in the loss model is explained. This is presented along with the performed simplifications and the code structure of the program.

Validation: The validation process is presented in this chapter, what program was used and how the simulations were performed. The result of the validation is also presented.

Results: The results from the area optimization of the loss model is presented. This is followed by a drivetrain optimization comparison between silicon IGBTs and SiC MOSFETs.

Discussion: The results of this thesis are discussed as well as the different obstacles encountered. A discussion about the limitations of the model is also presented along with thoughts on the drivetrain optimization comparison, and other applications.

Conclusion: Conclusions from the work in this thesis is presented along with thoughts on future work and possible improvements on the developed loss model.

II. Semiconductor and Modulation Theory

A. Semiconductor devices

Since the introduction of the transistor in 1947 [9], the ability to control and use electricity has improved rapidly. One of the developed applications are different power conversions such as DC to AC or AC to DC. Before the transistor was invented this could only be done with rotary converters, and later in the beginning of the twentieth century vacuum tubes [9]. With modern technology three phase converters can be produced with an efficiency of over 97 $\%$ [10]. Today the majority of the traction converters used in the automotive industry is using a Si IGBT based technology [11]. This technology has been developed greatly over the last few years and is dominating the automotive market [12]. One alternative to using IGBT converters is using MOSFET converters. When using a MOSFET converter, the freewheeling diode can be removed due to the reverse conduction capabilities of the MOSFET. When the freewheeling diode is needed, there are two possible solutions, either using a PiN diode, or a Schottky diode.

1) MOSFET: The power MOSFET is a semiconductor switch that was first introduced in the 1980s and is now well established. It is mostly used in applications with lower blocking voltage, usually $< 600\,V$ [13]. The MOSFET has three terminals labeled Source, Gate and Drain see Fig. 2. When the gate source voltage is lower than the gate source threshold, no current flows from drain to source. When a sufficient gate source voltage is applied, a conductive channel forms in the P+ regions, and current can flow through the MOSFET in either direction. The MOSFET is said to be in reverse conduction when current is flowing from source to drain, and the MOSFET supplied with a high gate source voltage. If a positive voltage, larger than the threshold voltage of the body diode, is applied across source drain on the MOSFET, a current flows. It does so, regardless of whether the gate source voltage is under or above the gate source threshold voltage, due to the PN junction formed in the MOSFET, marked as red diodes in Fig. 2. MOSFETs are the best choice for higher frequency applications, with moderate voltage $< 1000\,V$ [14]. However, if materials like SiC is used, higher voltages can be achieved due to the larger band gap energy of the material [15].

2) IGBT: The IGBT emerged also in the 1980s as a compromise between the high power bipolar junction transistor or BJT, and the MOSFET. It is now developed into much more than a compromise, with its high ruggedness, decent switching speeds and capability to withstand high blocking voltages, $< 6\,kV$ [13] [16]. The IGBT is a three terminal device as depicted in Fig. 3, with the terminals Gate, Collector and Emitter. Similar to the MOSFET the IGBT is controlled by an applied voltage over the gate emitter terminals [13]. This forms a conductive channel in the P regions in Fig. 3. If the gate emitter voltage is below the gate emitter threshold voltage no current can flow between collector and emitter. If a positive voltage is applied over emitter collector, no current flows regardless of the magnitude of the gate emitter voltage. The reason for this is the additional P+ layer in Fig. 3 compared to Fig. 2. This PN junction forms a diode that blocks current in this direction, assuming the emitter collector voltage is below the breakdown voltage. The IGBT typically has longer rise and fall time than the MOSFET [14].

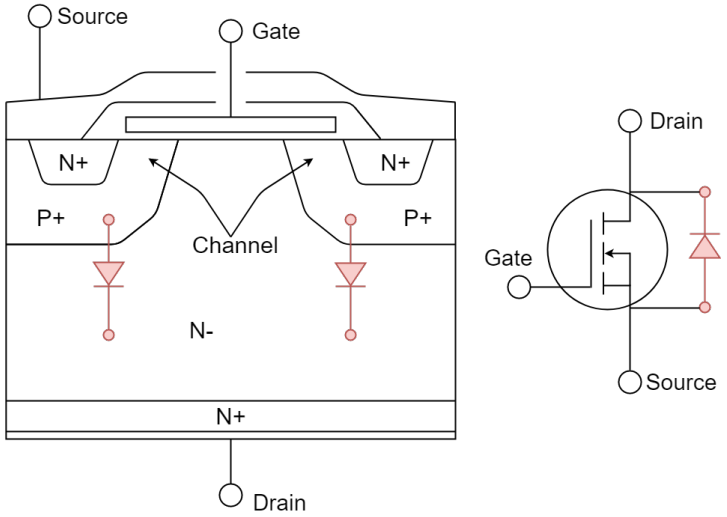

Fig. 2: Cross section of a power MOSFET, and the equivalent circuit symbol. When a positive voltage is applied to the gate, a channel is formed in the P+ region between the N+ and N-, and current can then flow from Drain to Source. The diodes in red are a parasitic result of the pn-junction formed in the MOSFET, which results in the MOSFET only being able to block voltage in one direction. The parasitic diodes can be used as freewheeling diodes in e.g. a three phase converter. (Note that the figure is not to scale, and so the actual relative size of the internal regions might not be correctly represented.)

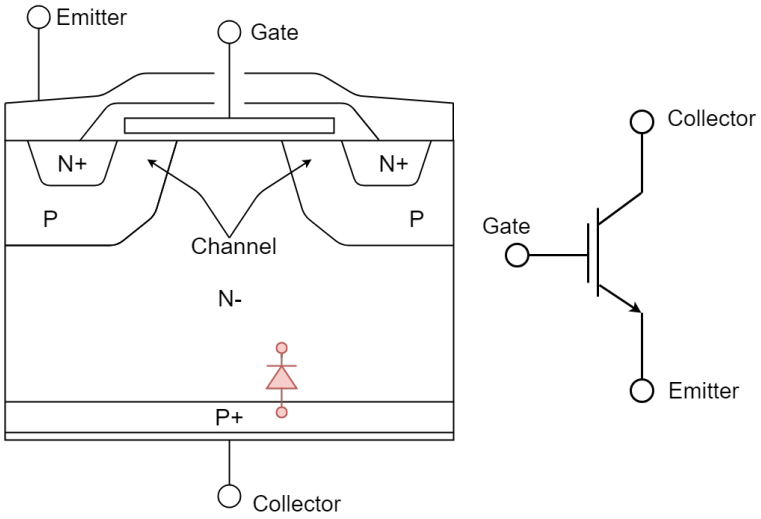

Fig. 3: Cross section of a power IGBT, and the equivalent circuit symbol. When a positive current is driven to the gate, a channel is formed in the upper P region between the N+ and N-, and current can then flow from collector to emitter. The diode in red is a result of the pn-junction formed in the IGBT, which results in that the IGBT only being able to conduct current in one direction. (Note that the figure is not to scale, and so the actual relative size of the internal regions might not be correctly represented.)

3) PiN Diode: The PiN diode is a semiconductor component that consists of a P-doped section, an intrinsic section and an N-doped section Fig. 4 [17]. When the diode is forward biased, the intrinsic region is filled with charge carriers from the P+ and N+ region. This leaves the intrinsic region with a carrier concentration several orders of magnitude higher than without the bias. At lower frequencies the PiN diode is similar to a regular PN juntion. During forward bias the PiN diode can be modeled as a resistance in series with an inductor. In reverse bias the PiN diode can be modeled as a capacitor in parallel with a resistor, both in series with an inductance [17]. The resistance in the forward biased model is low in comparison to the resistance in the model for reverse bias.

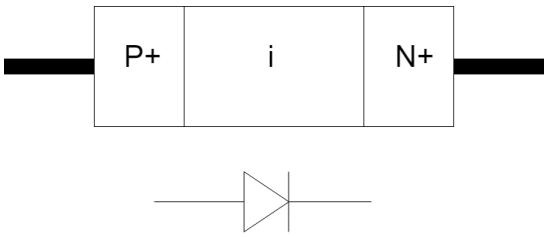

Fig. 4: Schematic representation of the PiN diode. It consists of a P+ doped section, an intrinsic section and an N+ doped section.

4) Schottky Diode: The low forward voltage drop and the fast switching capabilities is what truly makes the Schottky diode stand out [18]. It is well established with over 25 years in the power supply industry [18]. It is constructed from a N+ doped layer, a N- doped layer and a metal semiconductor contact Fig. 5, with a forward voltage ranging from 150 mV to 450 mV [18]. The first SiC component commercially available on the market was a SiC Schottky diode. The SiC Schottky diode was the first Schottky diode to have a breakdown voltage over 1000 V, before it was limited to under 200 V [15]. The SiC Schottky diode voltage drop is however higher than its silicon counterpart, rendering the component more suitable for high voltage application where the forward voltage drop has a smaller impact on the losses [15].

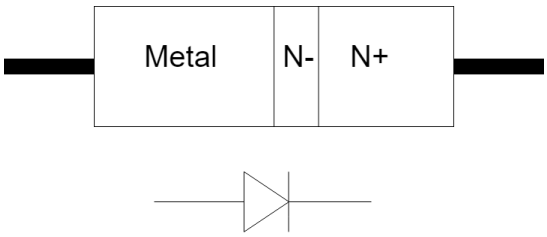

Fig. 5: Schematic representation of the Schottky diode. It consists of a metal section, an N- doped section and an N+ doped section. What is called a Schottky barrier is formed between the metal layer and the N- doped layer.

5) Silicon: Silicon is the most commonly used semiconductor for rectifiers and switches. Since it is so well established and the production methods are well refined, it's hard to compete with the low cost of silicon. A semiconductor is much more resistive than a conductor and can only be used as a conductor after doping. Silicon can for example be doped with Boron[19] or Phosphorus[20] to create the P and N regions respectively in a MOSFET Fig. 2.

6) Silicon Carbide: First discovered in 1891 by Edward G. Acheson, he was astonished by the great hardness of Silicon Carbide. Until 1929 it was actually the hardest synthetic material known to man. It is still appreciated for this quality, but lately more so for its semiconductor properties. It is used in sandpapers and cutting tools but the semiconductor qualities along with its thermal characteristics have inspired SiC switches [21]. The silicon carbide die of a transistor is thinner than that of a silicon die and doped to much higher levels which leads to lower losses[15]. Depending on the polytype crystal structure of silicon carbide, the energy gap of the material varies from 2.2 to 3.3 eV, which is 2 to 3 times higher than for silicon [15]. Technologically the polytypes 4H and 6H are of interest since from these it is possible to produce large wafers to cut components from [15]. The superior temperature characteristics can be demonstrated by observing the change in on state resistance of a SiC MOSFET compared to the Si counterpart. With a temperature increase from $25°\text{C}$ to $135°\text{C}$, the on state resistance of the SiC MOSFET increases approximately 20%, whereas that of the Si MOSFET increases 250% [15].

B. Semiconductor Losses

The switching losses for an IGBT and a MOSFET are given by the same equation (1)

$$P_{sw} = (E_{on} + E_{off}) f_{sw} \tag{1}$$

Where E_{on} and E_{off} are the switch on and switch off energies respectively. f_{sw} is the switching frequency of the semiconductor switch [22] [23].

The switching losses are, as the name suggests, a result of the switching of the transistor. During the switch, there is a voltage over the switch at the same time that it is conducting, which leads to power losses [13]. This is illustrated during $T_{sw(on)}$ and $T_{sw(off)}$ in figure Fig. 7. During the time the transistor conducts losses are produced due to the current that is flowing through the transistor. [13].

If the body diode of the MOSFET is used as a freewheeling diode additional reverse recovery losses are added to the switching losses according to (2).

$$P_{sw} = f_{sw}(E_{sw} + E_{Drr} + E_{Trr}) \tag{2}$$

Where E_{Drr} is the turn on energy of the diode. The turn on energy mostly comes from the reverse recovery charge and the turn off energy has been neglected (3) [22]. E_{Trr} is the reverse recovery energy, caused by the removing of the minority carriers in the internal diode. This current goes through the MOSFET and causes additional power losses (4) [22] Fig. 7. E_{sw} is the sum of E_{on} and E_{off} from (2).

$$E_{Drr} = Q_{rr}V \tag{3}$$

$$E_{Trr} = \frac{1}{4}Q_{rr}V \tag{4}$$

The actual E_{Drr} is calculated with Q_{rr} multiplied with the applied voltage over the transistor, however for worst case calculations this can be replaced with the battery voltage [22]. These additional switching losses need to be added since the switching loss curve in the datasheet comes from measurements with a test circuit with a Schottky diode as FWD Fig. 6. This means that no reverse recovery charge is present in the values in the datasheet.

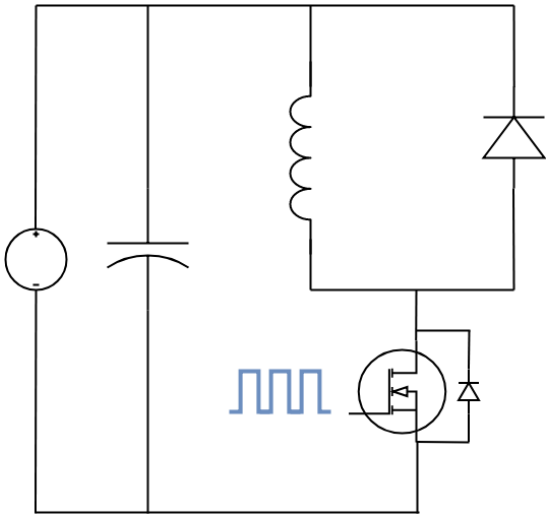

Fig. 6: The test circuit presented in the datasheet which shows that testing is performed with parallel Schottky diode [24].

The total switching losses of the MOSFET are given by (5) if the body diode is used as the freewheeling diode.

$$P_{sw} = f_{sw}(E_{sw} + Q_{rr}V + \frac{1}{4}Q_{rr}V) \tag{5}$$

The MOSFET conduction losses are given by (6) since it is modeled as a resistor during conduction [22]

$$P_{condM} = R_{ds}I^2_{Mrms} \tag{6}$$

where R_{ds} is the drain source on state resistance and I_{Mrms} is the rms current through the MOSFET.

The conduction losses for the IGBT can be described by (7), since it is modeled with a DC voltage source, representing the IGBT on-state zero-current collector-emitter voltage in series with a resistance [22] [23].

$$P_{condI} = V_{CE} I_{CEavg} + R_{CE} I_{CErms}^2 \tag{7}$$

V_{CE} is the IGBT on-state zero-current collector-emitter voltage. I_{avg} is the average current through the IGBT, R_{CE} is the IGBT on state resistance. I_{CErms} is the rms current through the IGBT. The conduction losses are illustrated in Fig. 7.

The conduction losses for the freewheeling diode can be described by (8) regardless of the diode being a PiN or a Schottky. The diode equation originates from a model of a DC voltage source in series with a resistance, representing the threshold voltage V_D and the forward resistance R_D of the diode.

$$P_{condD} = V_D I_{Davg} + R_D I_{Drms}^2 \tag{8}$$

I_{avg} is the average current through the diode and I_{Drms} is the rms current through the diode.

The total losses for a three phase converter are given by the sum of the switching and conduction losses of all transistors and diodes. (9) resistance[22] [23].

$$P_{tot} = P_{sw} + P_{cond} + P_{condD} \tag{9}$$

Where P_{sw} is either given by (1) or (5) depending on whether an external freewheeling diode is used or not. When using IGBTs for driving an inductive load the free wheeling diode is always needed. P_{cond} is the conduction losses of either the MOSFET or the IGBT and P_{condD} is the conduction losses of the external freewheeling diode if used.

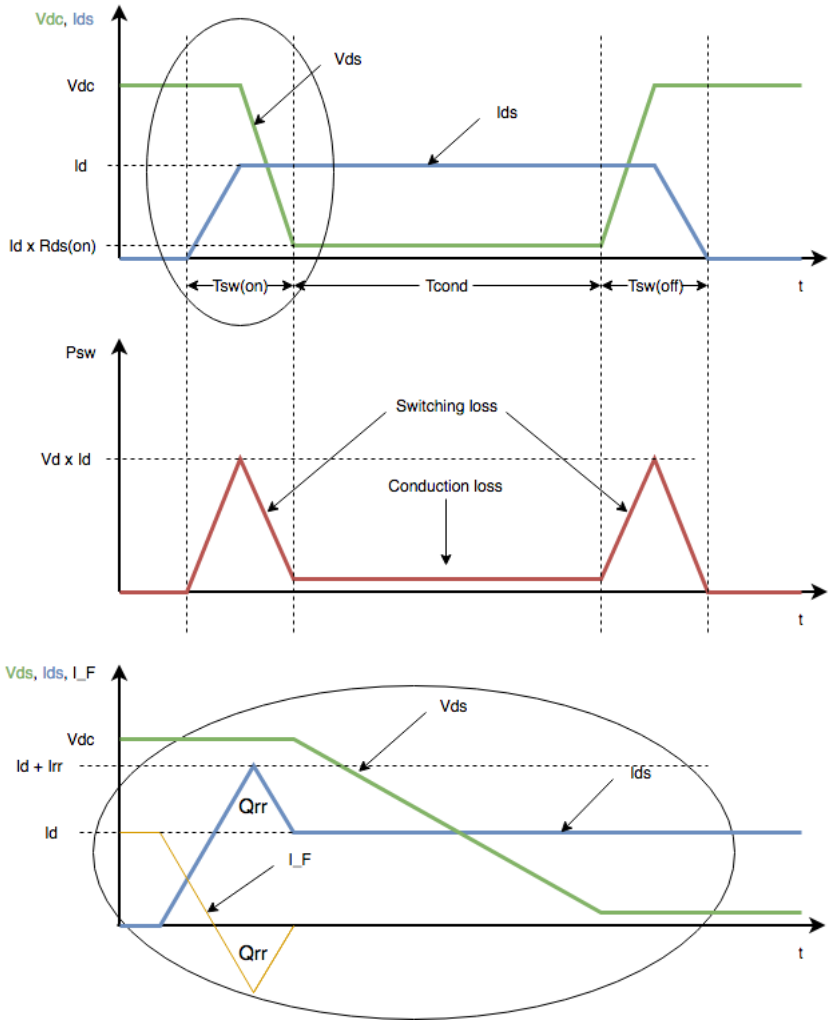

Fig. 7: Switching waveforms for a MOSFET (top figure). When the switch is turned on, the drain-source current starts to flow before the voltage has dropped, this gives rise to power loss (middle figure). I_F is the forward current of the internal diode. Irr is the peak reverse recovery current caused by the minority carriers in the internal diode. Qrr is the reverse recovery charge (bottom figure). Figure inspired by [22].

C. Thermal Network

The following section is focused on the thermal modeling of a power module, but similar calculations can be used for discrete components. The power loss in a semiconductor leads to an increase in junction temperature, T_j. The magnitude of this temperature increase depends on a number of factors; what material the semiconductor component is fastened to, the thermal resistance of said material, the ambient temperature and the power loss of the semiconductor device. This is expressed in equation (10).

$$T_j = P_d R_{th} + T_a \tag{10}$$

where P_d is the power dissipation of the semiconductor device and T_a is the ambient temperature. The thermal resistance, R_{th}, is calculated from 11.

$$R_{th} = \frac{d}{\lambda A} \tag{11}$$

using the the thermal conductivity λ, area A and the material thickness d. If the semiconductor component is not connected directly to the heat sink but rather through different layers of materials, the thermal resistance of each layer acts as series connected electrical resistances and add up. An effective cooling structure allows for a greater power dissipation, allowing the semiconductor to operate at higher frequencies, currents and voltages without overheating. Combining (10) and (11) results in (12)

$$P_d = \frac{\lambda A \Delta T}{d} \tag{12}$$

which shows that to allow for a greater power dissipation, the goal is thin material layers with a high thermal conductivity, large areas and a low ambient temperature, where ΔT is T_j - T_a [25].

A simple two dimensional thermal model from junction to case is shown in Fig. 8. Each layer has its own thickness, area, and depending on the material of the layer, a thermal conductivity. With the geometrical complexity of heat sink designs, the thermal resistance is rather experimentally measured than calculated from (11). The heatsink can still be seen in Fig. 8. The thermal interface material, TIM, that connects the baseplate to the heat sink can also be seen and its R_{th} can also be calculated with (11). To accurately calculate the thermal resistance of the stack, the effective area of each layer has to be known. With the different materials having different thermal conductivities, the heat spread angle is also different and so the effective area for each layer becomes difficult to calculate by hand.

Using a finite element model, the total junction temperature can be simulated with a given ambient temperature and power dissipation. Thus the difficulties with the effective areas are eliminated. The thickness, area and thermal conductivity of each layer can be set to match specifications, the junction temperature is simulated and with (10) the total R_{th} can be calculated with the effective area of each layer taken into account.

The semiconductor chip is soldered or sintered to a copper track, and bond wires connect the chip to additional copper tracks. The ceramic is in place to provide electrical insulation between the potential at the power component and the potential at the cooling medium, while maintaining a high thermal conductivity. The ceramic can be made from different materials, which have different thermal conductivities which affect the R_{th} of the stack. The coefficient of thermal expansion also differs between different materials. If it differs too much from the adjacent layer, the thermal expansion can cause cracks and ultimately loss of function. The direct copper bonded substrate is soldered or sintered to the baseplate of the power module. To connect the power module to a heat sink, a TIM is applied. This is done to reduce the thermal resistance caused by air otherwise present between the baseplate and heat sink due to surface ruggedness.

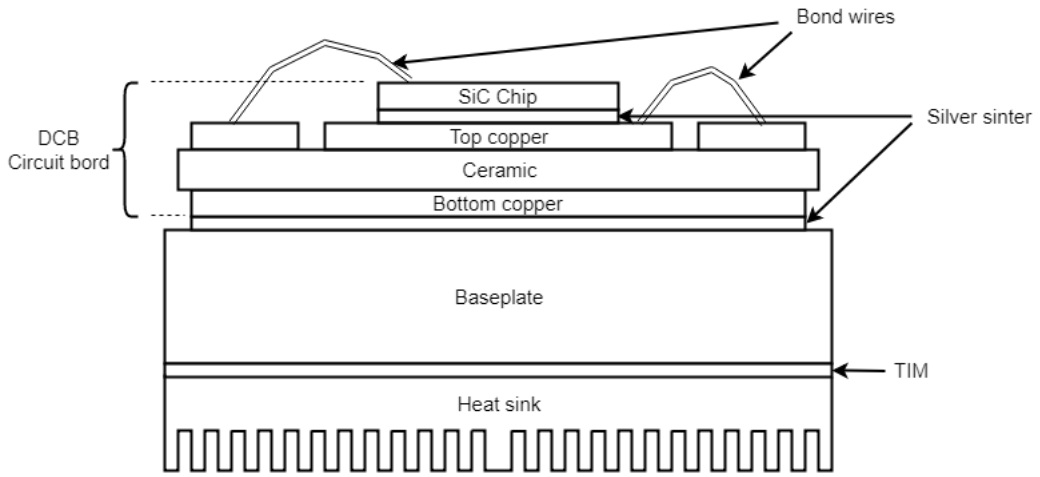

Fig. 8: The approximate geometry and materials of the thermal stack used in this model is shown here.

D. Gate Driver

To allow the six switches in Fig. 10 to have a synchronous three phase output, a circuit controlling the gate voltages of the switches is needed. That circuit is a modulator circuit along with the gate driver. For the switches to be able to operate according to the datasheets, the gate driver needs to fulfill some specifications. The required gate voltage of a MOSFET can be directly extracted from the datasheet. The required peak current I_{Gpeak} of the gate driver can be calculated with (13) [26]

$$I_{GpeakM} = \frac{Q_g}{dT} \tag{13}$$

where Q_g is the total gate charge and dT is the rise or fall time of the switch, whichever is the shortest. Rearranging (13) so that dT is isolated, it can be seen that there is a reason for the need of this peak current. I_{GpeakM} controls dT, should I_{Gpeak} be smaller, dT increases, rendering some datasheet values invalid. It should be noted that no current flows from the gate of the switch to either drain or source. The current from the gate driver is instead used to charge the gate capacitance.

The IGBT just like the MOSFET is a voltage driven transistor[27]. The peak gate driver current required for an IGBT can be calculated with (14)[28].

$$I_{GpeakI} = \frac{V_{G_{on}} - V_{G_{off}}}{R_g} \tag{14}$$

Where $V_{G_{on}}$ and $V_{G_{off}}$ is the turn on and turn off gate voltage respectively. R_G is the total IGBT gate resistance. One of the most popular and cost effective circuits of a gate driver for MOSFETs is shown in Fig. 9 [29].

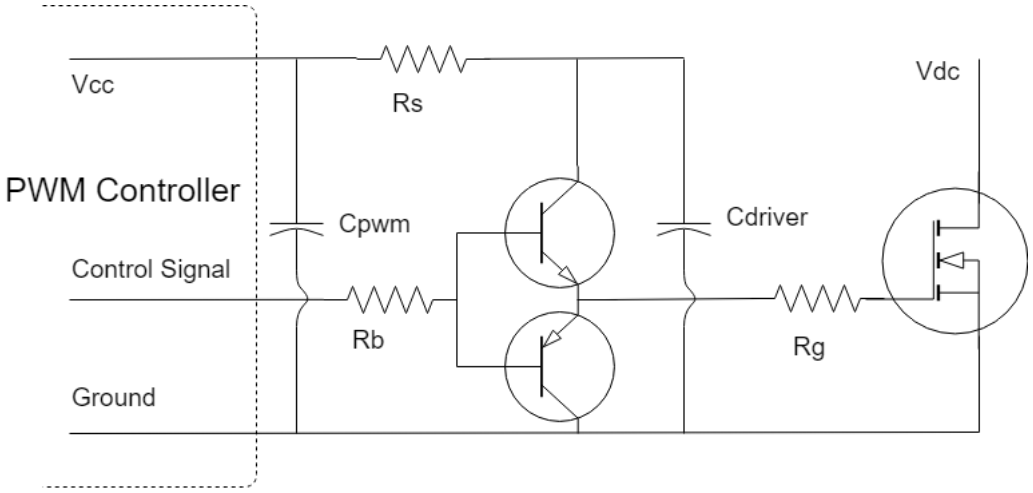

Fig. 9: The schematic for a popular gate driver circuit. R_s is a smoothing resistance between the driver bypass capacitance and the PWM controller bypass capacitance. R_b needs to be sized according to the driver transistors and R_g is optional [29].

E. Three Phase Converter

The purpose of a three phase converter is to create three phase AC power from a DC power source. The converter is constructed by using three half bridge legs as in Fig. 10, where each leg conducts one phase current for the three phase inductive load.

Every phase leg of the converter can be visualized as a switch, if the upper transistor is conducting the switch is considered to be ON and if the lower transistor is conducting the switch is considered OFF. By thinking of the converter in this way it is clear that eight different switch combinations are possible for the converter, this is visualized in Fig. 11.

If the first leg of the converter is ON, and the upper transistor is conducting in the positive direction, this means that a positive current I_R, is flowing via the upper transistor and out of the half bridge leg. Assuming that the lower switches are on in the other bridge legs, this means that they are conducting a current into those phase legs and via their lower transistors. This is equivalent to the switching state (1,0,0) in the upper right of Fig. 11. By using a variation of sinusoidal modulation schemes to turn on and of the switches a sinusoidal load current can be achieved for each phase. This is further explained in the upcoming chapter.

The DC-link capacitor in three phase converters is used as a load-balancing energy storage device. This helps to protect the converter from voltage spikes and other noise caused by the pulsed converter current [30]. In Table III the different switch states and the resulting load voltage is presented. The voltage U over the inductive load sets the current derivative according to (15).

$$u = L\frac{di}{dt} + R_L i + e_a \tag{15}$$

where L is the inductance of the load and i is the current through it, R is the resistance of the load and e_a is the generated back emf Fig. 10.

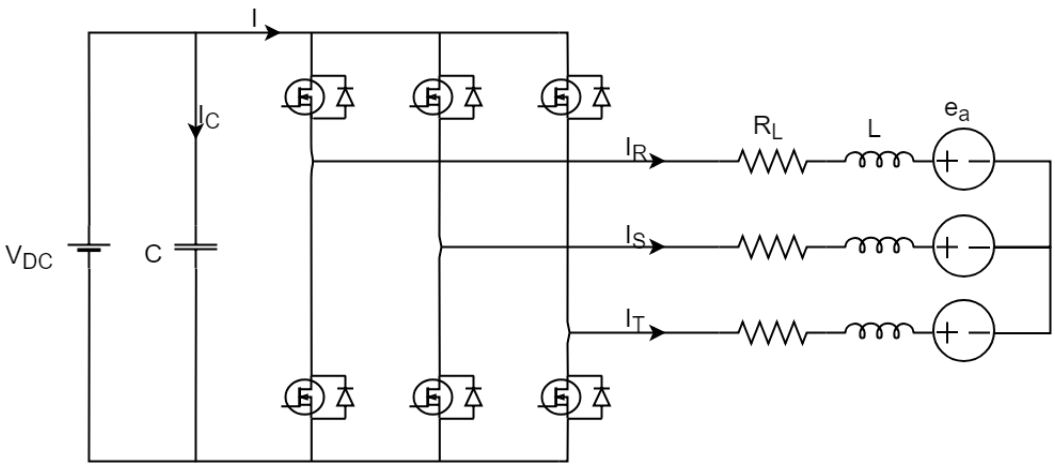

Fig. 10: Converter connected to DC source and Motor.

F. Modulation schemes

Modulation can be done in several different ways. The simplest, most straight forward modulation scheme is sinusoidal pulse width modulation or SPWM, without any zero sequence voltage component [31].

TABLE II: Voltage over phase load for phase R

Load voltage	**switch state**
2*Vdc/3	(1,0,0)
1*Vdc/3	(1,0,1), (1,1,0)
0	(1,1,1), (0,0,0)
-1*Vdc/3	(0,0,1), (0,1,0)
-2*Vdc/3	(0,1,1)

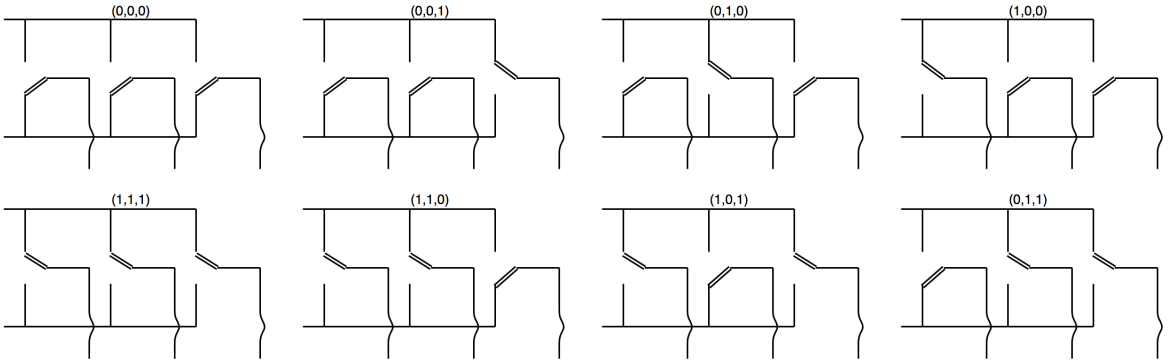

Fig. 11: The eight switch combinations of the three phase converter. Figure inspired by [13].

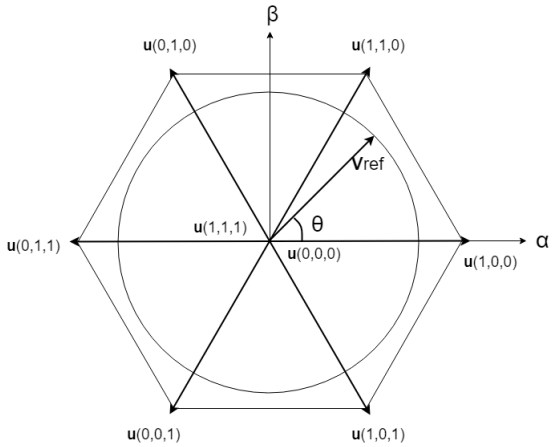

Fig. 12: The eight switch combinations of Fig. 11 represented as complex vectors in the $\alpha\beta$ domain. The Vref voltage vector represents the rotating motion of the output voltage of the three phase converter. The outer hexagon is the maximum output voltage. The circle is a possible route for the voltage vector for a given modulation speed and DC link voltage.

TABLE III: Output voltage vectors

Vector in $\alpha\beta$ domain	Corresponding switch state
$\sqrt{\frac{2}{3}}U_{DC}$	(1,0,0) & -(0,1,1)
$\sqrt{\frac{2}{3}}U_{DC}e^{\frac{j2\pi}{3}}$	(0,1,0) & -(1,0,1)
$\sqrt{\frac{2}{3}}U_{DC}e^{\frac{j4\pi}{3}}$	(0,0,1) & -(1,1,0)
0	(0,0,0) & (1,1,1)

By altering the shape of $v_{N_{ref}}$ it is possible to achieve a higher modulation index than one and still have linear modulation. This is done by adding zero sequence signals to $v_{N_{ref}}$. Two other ways are SPWM with symmetrical modulation and bus-clamped modulation. These different modulation schemes correspond to different $v_{N_{ref}}$ in Fig. 13. All of them can be thought of as sinusoidal modulation schemes, but symmetrical and bus-clamped modulation has an added zero sequence current, which changes the appearance of $v_{N_{ref}}$ [13]. The zero sequence current is added by adding the same signal on to $v_{N_{ref}}$ of each phase. These methods are used to reduce the switching losses and the harmonic content in the output signal [31]. From here on sinusoidal modulation is assumed. With the right switching scheme for the converter, a three phase system can be achieved with every phase current shifted 120° apart. Theoretically, one of the switches in every converter leg is always conducting. However in real applications the active switch is shut off just before the non active switch is turned on to avoid a short circuit. The time between these two switches is called blanking time. Two different SPWM schemes are presented here.

1) MFD: In this modulation scheme, reverse conduction is prevented. The gate driver output voltage is kept low during freewheeling. The result of this is that the freewheeling current is forced through an external Schottky diode. This behavior can be seen in Fig. 13 c.

2) MRC: In this modulation scheme, the gate voltage follows the behavior of MRC in Fig. 13. In this scheme the reverse conduction capabilities of the MOSFET are utilized. The freewheeling current is split between the MOSFET and an external Schottky diode.

The modulation index M can be defined as (16) for sinusoidal modulation.

$$M = \frac{\hat{V}_{N_{ref}}}{\hat{V}_{cw}} \tag{16}$$

where $\hat{V}_{N_{ref}}$ is the peak value of the reference wave, and $\hat{V}_{cw}$ is the peak value of the carrier wave Fig. 13. With sinusoidal modulation, the maximum modulation index that can be achieved, is one.

G. Derivation of Component Currents

When performing loss calculations on an converter, the current through the transistors and diodes is what causes the losses. In the example with an converter as a motor drive, these currents do not correspond to the 3-phase rms currents of the motor (17) but rather the specific currents through the components.

$$I_{N,rms} = \frac{P_{3-phase}}{\sqrt{3}V_{LL}PF} \tag{17}$$

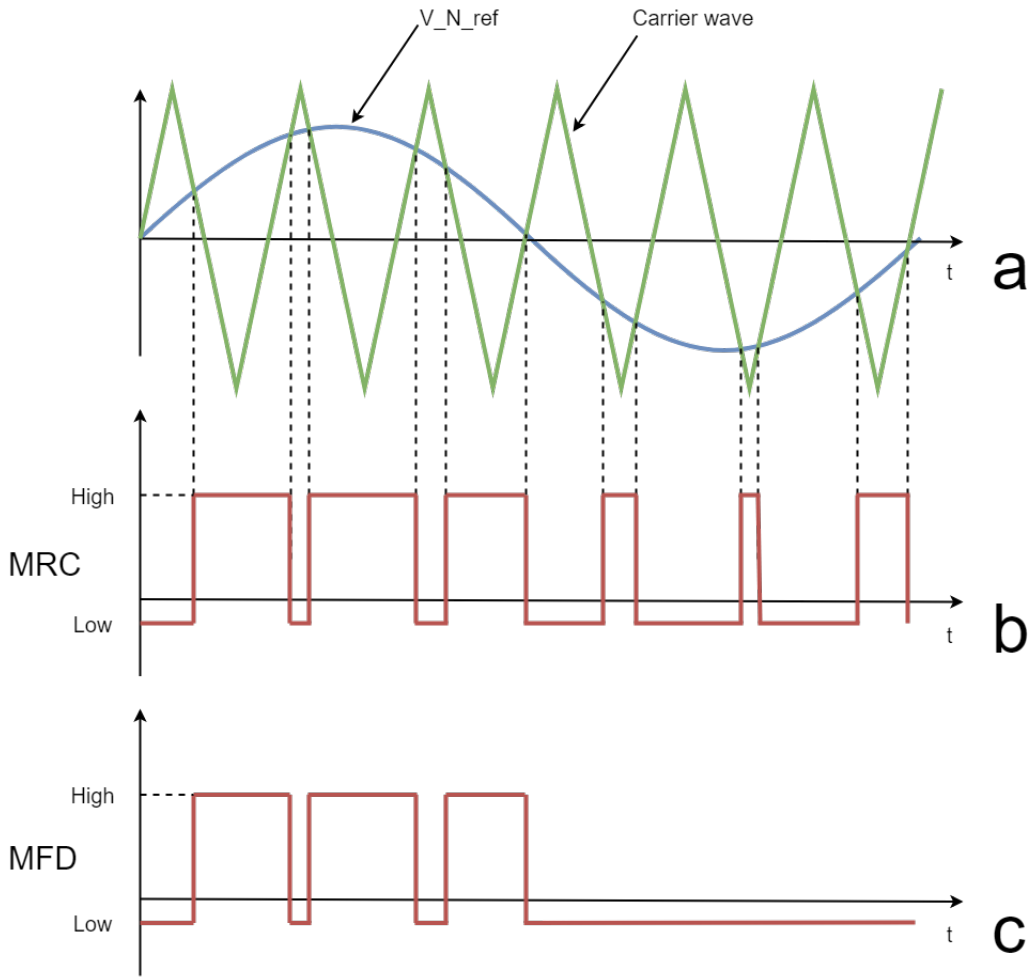

Fig. 13: PWM modulation diagram for the upper switch in every phase leg. The upper diagram shows the signals in the gate driver. The lower two diagrams shows the gate driver outputs for the two different modulation schemes. When $v_{N_{ref}}$ is bigger than the carrier wave the output voltage is high. If the opposite is true then the output voltage is low. The inverse behavior is true for the gate driver of the lower switch in the same phase leg. The frequency of the carrier wave is in reality much greater than the frequency of $v_{N_{ref}}$ but is lowered in this figure for visibility.

1) MFD: The MFD case is when the modulation scheme of the converter is so that the reverse conduction is not utilized but instead the freewheeling current is handled by an external diode. This is shown by the black line in Fig. 14. The same as for the previous case applies, the body diode of the MOSFET conducts if the current is large enough, i.e when the external freewheeling diode voltage drop forward biases the internal diode.

The derivation of the currents for MFD are shown below. The peak value of a single phase current is denoted I_0 which equals $\sqrt{2} \times I_{N,rms}$ [22]. The time dependent phase current I_N is given by (18).

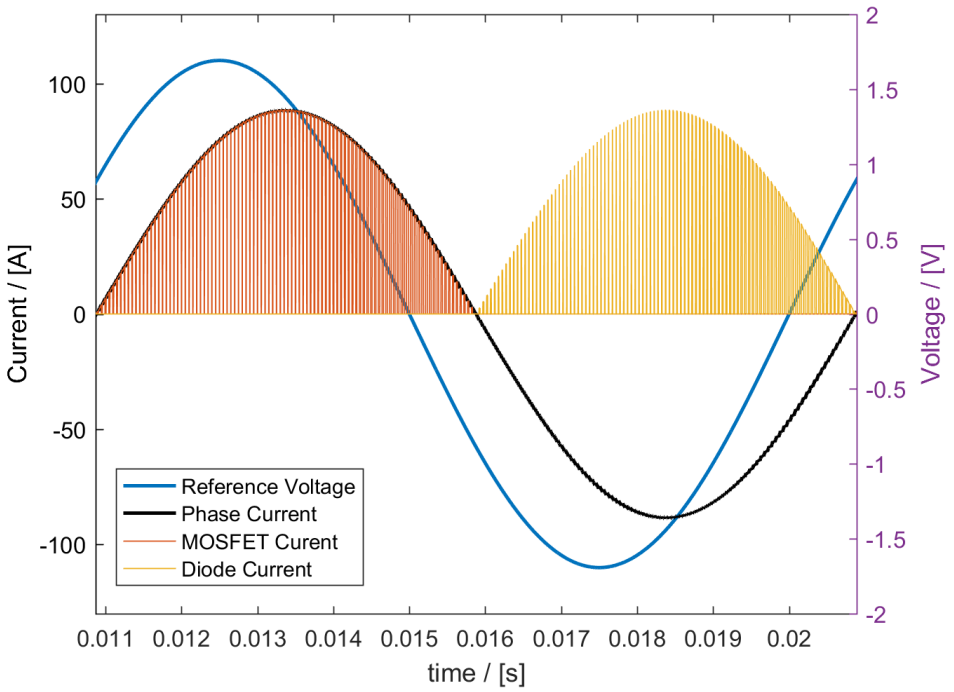

Fig. 14: Using MFD the resulting current and voltage curves for the upper switch look like in the LTspice simulation above. The data from the simulation is transfered to MATLAB for clarity. The resulting phase current can be seen as the black line, the upper MOSFET current is the red pulsed area in the first half period and the upper diode current is the yellow pulsed current in the second half period.

$$I_N = I_0 sin(\alpha - \phi) \tag{18}$$

where α is the time dependent variable and ϕ is the phase shift. The function for the duty cycle δ is given in (19)

$$\delta = \frac{1}{2}(1 + Msin(\alpha)) \tag{19}$$

where M is the modulation index for δ. It is assumed that the frequency of the carrier wave is much greater than the fundamental frequency of the reference voltage Fig. 13. The transistor rms current and the transistor average current can be calculated by integrating the phase current multiplied by the duty cycle δ according to (20) and (21).

$$I_{RMS} = \sqrt{\frac{1}{2\pi}\int_{\phi}^{\pi+\phi}(I_N^2\delta)d\alpha} \tag{20}$$

$$I_{Ave} = \frac{1}{2\pi}\int_{\phi}^{\pi+\phi}(I_N\delta)d\alpha \tag{21}$$

To calculate the diode currents (23) and (25) one would replace δ by $1-\delta$ in (21) and (20).

The rms value of the transistor current is given by (22) [22]

$$I_{rmsT} = I_0\sqrt{\frac{1}{8} + \left(\frac{Mcos(\phi)}{3\pi}\right)} \tag{22}$$

Similarily the current through the diode is given by (23) [22].

$$I_{rmsD} = I_0\sqrt{\frac{1}{8} - \left(\frac{Mcos(\phi)}{3\pi}\right)} \tag{23}$$

The average currents are calculated with (24) and (25) [22]

$$I_{AveT} = I_0\left(\frac{1}{2\pi} + \frac{Mcos(\phi)}{8}\right) \tag{24}$$

$$I_{AveD} = I_0\left(\frac{1}{2\pi} - \frac{Mcos(\phi)}{8}\right) \tag{25}$$

2) MRC: The MRC case is the most complicated case from an analytic calculation perspective. The reverse conduction of the MOSFET is used in parallel with an external Schottky diode. A visualization of the current split between the diode and the MOSFET can be seen in Fig. 15. Reverse conduction can according to [32] decrease the total losses of the converter up to 16.7% percent.

Intuitively, MRC would also mean increased switching losses but since the diode is conducting in parallel and during blanking time, the voltage is forced to $V_d + R_d I_o$, this means that the entity of the switching losses are negligible [33]. During the part when the MOSFET is conducting on its own, the current through the MOSFET is given by (26) [33].

$$i_{M1} = I_o sin(\alpha - \phi) \tag{26}$$

By modeling the current split as in the equivalent circuit in Fig. 16 the time dependent MOSFET- and diode currents during freewheeling can be derived as 29 and (30).
Kirchoffs current law for node V1 gives 27

$$\frac{V1 + Vd}{R_d} + \frac{V1}{R_{on}} - I_o sin(\alpha - \phi) = 0 \tag{27}$$

where solving for V1 gives 28.

$$V1 = \frac{R_{on}R_d I_o sin(\alpha - \phi) - R_{on}V_d}{R_{on} + R_d} \tag{28}$$

With the voltage in V1 it is trivial to calculate the currents through the MOSFET(29) and the diode(30).

$$i_{M2} = \frac{R_d I_o sin(\alpha - \phi) - V_d}{R_d + R_{on}} \tag{29}$$

$$i_D = \frac{R_{on} I_o sin(\alpha - \phi) + V_d}{R_d + R_{on}} \tag{30}$$

β is defined as the angle between when the MOSFET starts reverse conducting on its own, until the diode starts conducting in parallel Fig. 15. The rms currents can be derived by integrating the MOSFET and

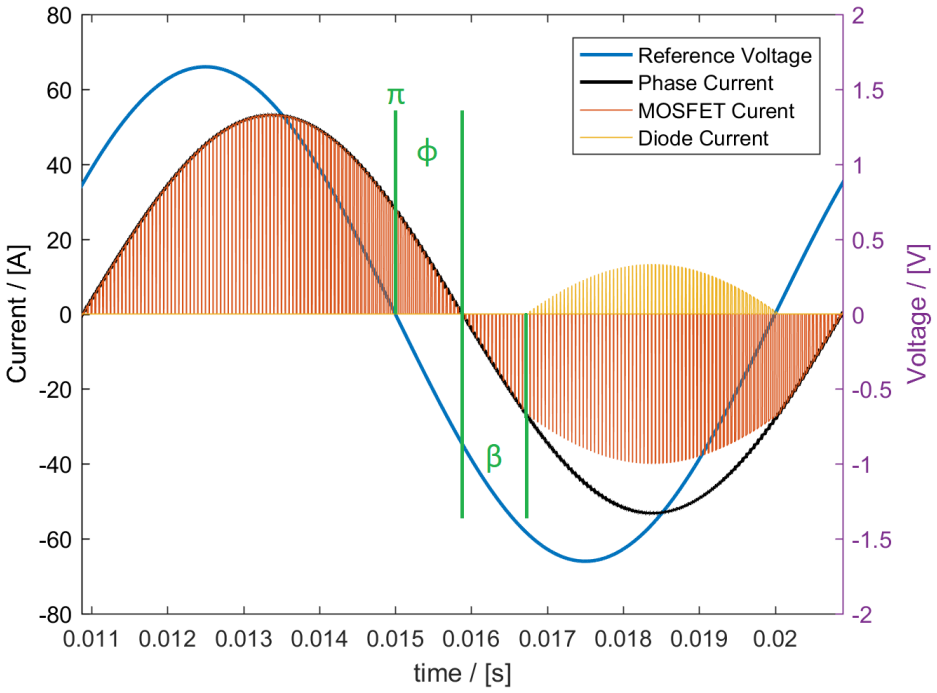

Fig. 15: Using MRC where reverse conduction is utilized the Schottky diode and the MOSFET shares the current during the second half period leading to the appearance seen in the graph. β is the phase difference between when the diode starts conducting and the MOSFET starts conducting in reverse conduction and ϕ is the phase difference between voltage and current.

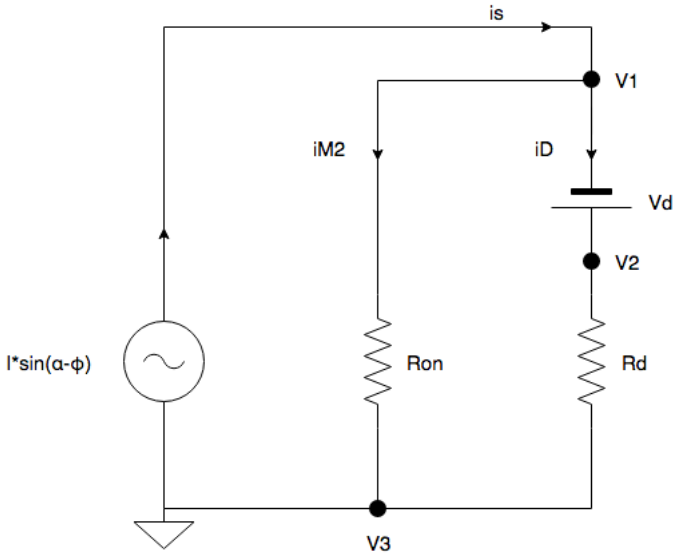

Fig. 16: The equivalent circuit for calculating the current split during reverse conduction.

diode currents multiplied by δ according to (31) and (32) [33]. Only the MOSFET is conducting during the period from ϕ to ϕ+π as can be seen in Fig. 15. The diode is also conducting during ϕ+π to ϕ+π+β and from ϕ+2π-β to ϕ+2π. From ϕ+π+β to ϕ+2π-β the MOSFET and diode are conducting in parallel.

The final expression for the MOSFET and diode rms current is then given by calculating the integrals 31 and 32 [33]

$$i_{Mrms} = \sqrt{\frac{1}{2\pi}\int_{\phi}^{\phi+\pi+\beta}(\delta)\Big(i_{M1}\Big)^2 d\alpha + \frac{1}{2\pi}\int_{\phi+\pi+\beta}^{\phi+2\pi-\beta}(\delta)\Big(i_{M2}\Big)^2 d\alpha + \frac{1}{2\pi}\int_{\phi+2\pi-\beta}^{\phi+2\pi}(\delta)\Big(i_{M1}\Big)^2 d\alpha} \tag{31}$$

$$i_{Drms} = \sqrt{\frac{1}{2\pi}\int_{\phi+\pi+\beta}^{\phi+2\pi-\beta}(\delta)\Big(i_{D}\Big)^2 d\alpha} \tag{32}$$

To calculate the conduction losses for the diode the diode average current is needed, this is given by (33) [33].

$$i_{Davg} = \frac{1}{2\pi}\int_{\phi+\pi+\beta}^{\phi+2\pi-\beta}(\delta)\Big(i_{D}\Big) d\alpha \tag{33}$$

The results of (31), (32) and (33) can be seen in Appendix B.

3) Internal Body Diode: This case is not implemented in the optimization program. The component currents interact differently depending on the modulation scheme and design of the converter. In the most simple case, design wise, there are no external free wheeling diodes and the converter is modulated so that conduction through the internal body diode is used. This case showed little promise in terms of efficiency and is therefore neglected in the optimization program. While the converter currents are negative, only the reverse body diode current is present (34). The modulation method utilizing the internal body diode has the same current derivation as using MFD. The difference being that the thermal development is present on the MOSFET instead of a external diode.

$$I_{rmsT} = I_{N,rms} \tag{34}$$

III. Method

The initial phase of this project was to perform literary studies on the most relevant semiconductor technologies, and to choose one of these to be the main focus of the project. The second phase consisted of getting familiar with the structure and necessary inputs to the optimization model. After this the implementation of the area optimization loop was made, followed by validation of the data to make sure the model output gave reasonable results.

A. Literature study

Before this master thesis was started a literature study was made. It started with participating in a workshop that was held by the creators of the previously mentioned DTOP. This gave an overview of the way they had worked to develop this software as well as a basic understanding of the software itself and it's different components.

The thesis work was started by looking into different semiconductor technologies that was on the horizon for PE applications. SiC and Gan were the most well researched materials as replacements for Si [34] [35], where SiC is especially suitable for HV applications and high switching frequency applications [36]. Si is the material with the widest application spectrum, while SiC and GaN has more specific uses, but show promising results in the PE area [36]. The use of SiC would according to [3] allow a reduction of motor losses due to the possible increase of switching frequency. This further motivated the choice of semiconductor material. Silicon carbide was chosen as the semiconductor technology for this project.

The next step in the process was understanding the area optimization loop and loss estimation that is used in the original DTOP [5]. This included finding out which input parameters that would be available, what output parameters was needed for the rest of the optimization, as well as understanding the area optimization design and principles used. This is important to be able to create an area optimization that gives a result comparable with the Si model made for the original software.

It was important to make sure there was enough data available, for both SiC MOSFETs and SiC Schottky diodes, to be able to make a loss model that would work within a desired range of currents. The bare die datasheets for the MOSFETs turned out to be the most rare, and these were vital to be able to optimize the area of the MOSFET in respect to temperature and current. Wolfspeed turned out to be the only company that was providing enough data to be able to relate the bare die area with the current I_{ds}, and therefore these were chosen as a base for the SiC loss model.

It was made sure that there was enough data available for choosing SiC as the semiconductor material for this thesis. A study of different ways to calculate losses for transistors and diodes was made [22] [23]. A short comparison was made with the original optimization model for Si to make sure that the loss models were on a similar level of detail and accuracy. The modeling of different current splits is discussed in [33] and [37]. The MRC current split is also discussed and verified with simulations in [38]. The MFD current split was derived from the loss formulas in [22] [23].

A loss model of sufficient detail was chosen for each of the semiconductor devices. The datasheets for the SiC devices were inspected again, this time in search for parameters that could effect the loss models. It was found that the semiconductor power losses had temperature dependencies [39] that were neglected in the original formulas. These dependencies were included in the loss calculation formulas to better match the behavior seen on the datasheets.

B. Area optimization design / architecture

When the literature studies were considered done the implementation of the optimization programs was started. This section describes the steps taken through the project to realize the optimization model and describes them in a general fashion. This is further explained and discussed in following chapters.

1) Input and output parameters: To know how to approach the implementation of the optimization, the input and output parameters needed to be known. Once the input parameters were known, loss models could be generated together with the device datasheets, to generate the desired output parameters. The final output parameters would be the total semiconductor cost and area of a three phase converter.

2) Map and function generation: Relevant data was extracted from the datasheet diagrams for SiC MOSFETs, including the internal diode as well as for SiC Schottky diodes from Wolfspeed. This data was then re-constructed in MATLAB to recreate the plots in the datasheets. In some cases where there was enough data, an additional dependency was added, for example temperature dependencies. When plots and maps where made they where interpolated to functions to be able to extract data seamlessly from between the extracted data.

The raw data gathered from datasheets, was digitalized using the MATLAB program Grabit. Grabit allows a user to load an image of a graph, pinpoint the minimum and maximum of the x- and y-axis, and then to pinpoint any number of points on a curve in the graph. The program outputs a n-by-2 matrix where n corresponds to the number of values that were pinpointed on the graph and the two columns are the x and y values. The matrix can be opened and used in MATLAB.

Since the optimization is made based on the area of the semiconductor device, it was vital to find how the losses for each device depended on the area. That means that an area dependency can be found in most functions describing the behavior of the semiconductor components.

3) Loss calculation: The generation of the maps made the loss calculation more straight forward. The total losses are given by (9). Since the switching frequency is an input parameter for the model, the total switching losses for each optimization loop is calculated by taking the E_{sw} for the actual current and area from the map and multiplying with the switching frequency (35). The conduction losses are calculated with (6) and (8) in each loop by extracting the forward resistance of the MOSFET or the diode from a map, based on area and temperature. The threshold voltage of the diode comes from a function only dependent on temperature, and the currents for the conduction losses are constant input parameters.

4) Thermal model: When the model was finished for the losses of the semiconductor devices, a thermal model was needed to calculate the resulting change in temperature. The output of the thermal model is $R\Theta_{ja}$. An area dependent FEA was performed in Comsol to calculate the total thermal resistance of the stack. With thickness, area, thermal conductivity for each layer, a predetermined ambient temperature and a fixed power dissipation, the junction temperature can be calculated with the FEA. From this the total thermal resistance can be calculated with (10). A two dimensional blueprint of the thermal model can be seen in Fig. 8. the calculated junction temperature is used for comparison with the maximum allowed temperature for the converter in the optimization loop.

5) Optimization loop: When all the preparatory models were made, the optimization program was implemented. It was implemented using a main script to first create all the constant input parameters, and then call the other scripts to initialize all the needed data to be able to run the optimization. After this, an optimization loop as described in Fig. 35 is run. Here, a comparison is made between the calculated and the maximum allowed junction temperature and the area is adjusted accordingly.

6) Parallel semiconductor devices: The maps made earlier in the process are limited to the available datasheet data and area and therefore limited in their current handling capabilities. The currents for the application of a motor drive converter are in reality higher than the maximum current in available datasheets, therefore a function to connect the components in parallel was developed. This function is explained in Fig. 34. It results in the area optimization made for a single component being able to handle many components in parallel as well, which is needed to be able to handle a large total current.

7) Optimization reverse conduction: To be able to utilize the reverse conduction capabilities of the MOSFET another type of optimization is implemented. A matrix of different area and different amount of parallel devices is run through the loss estimation and thermal model script to create a matrix of different temperatures for each area combination. The valid temperatures, that are below the maximum allowed are sorted out from the rest and then these values are searched for a minimal cost.

8) Complete converter: The area for all the semiconductor devices are added together to give a total estimate of the size of the converter needed for the system. The diode and MOSFET area, together with the respective cost per square millimeter quote gives a total cost for semiconductor area.

C. Validation

For validation of the different current splits implemented in the loss model corresponding to the two different modulation schemes, a three phase converter model was created in the circuit simulation program LTspice. The resulting currents of the loss model were validated, by running the LTspice with the same input parameters, and comparing the magnitudes of the resulting currents. This process is explained in more detail in the validation chapter.

IV. Modeling and Optimization

The losses of the different semiconductors used in the optimization program need to be modeled based on their physical characteristics and operating points to be able to determine their optimal size for a given application. To be able to give a fair estimation of the losses and the thermal calculations, and still stay within reasonable depth of the analysis, some limitations and simplifications are done. Simplifications were also performed due to limited data. In some cases several choices of approach were possible and in this section these simplifications, limitations and choices of approach is presented and motivated. To clarify the difference between using reverse conduction or exclusively diodes for freewheeling, the reverse conduction case is called MRC and using diodes exclusively for freewheeling is called MFD.

A. Switching losses

To calculate the total switching losses in (1) E_{sw} needs to be modeled with correct dependencies. In this thesis E_{sw} (35) is modeled as $E_{sw}(I, A, T)$ where the current and area dependent switching energy is taken directly from the datasheets of the devices and the temperature dependency is added as a factor normalized around $25°C$.

$$E_{sw} = E_{sw}(I, A, T)\left(\frac{V_{DC}}{V_{ref}}\right)^{k_v} \tag{35}$$

V_{DC} is the applied DC-link voltage and V_{ref} is the reference voltage for which the switching losses are given in the datasheet. k_v is a compensation factor for eventual DC-link voltage differences where the factor is normalized around an applied blocking voltage of 800V. This factor is calculated from datasheet values for the voltage. This is explained further below.

The switching energy E_{sw} is given directly in the datasheets and consists of the switch-on and switch-off energies E_{on} and E_{off}, at a junction temperature of 25° C and a DC-link voltage of 800V. This can be seen in the left graph in Fig. 17 below.

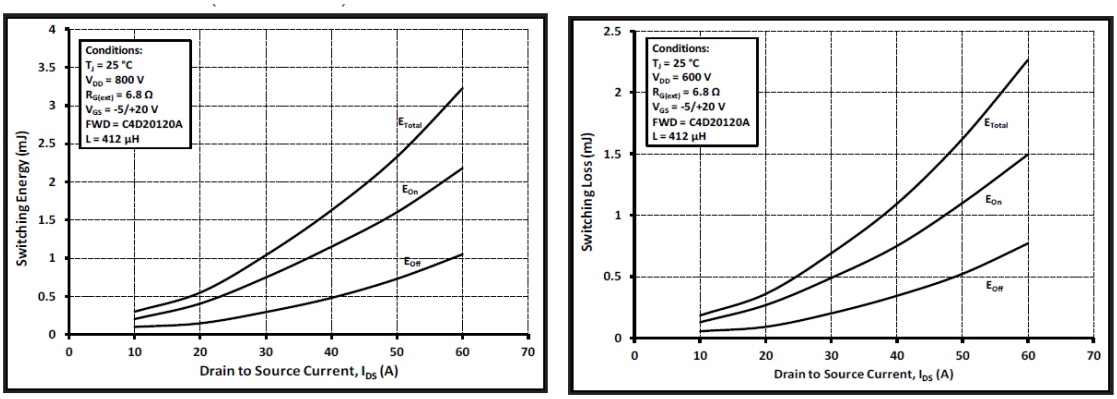

Fig. 17: Switching losses given from datasheet for the 25 Ω R_{ds} rated MOSFET from Wolfspeed [24]. To the left is the switching energy curve for a blocking voltage of 800 V and to the right is the equivalent curve for 600 V.

By combining these graphs with corresponding area-data from bare die datasheets, a surface is created that gives the switching losses for any given combination of area and current as seen in Fig. 19. This data is given for a junction temperature of 25 °C and therefore a temperature compensation is needed to get the correct losses for the given combination. By taking the data from the curves in Fig. 18 below and interpolating the points taken, the curves can be recreated and a second degree polynomial is fitted

to the function. Only one temperature setting can be used for each map and for the final map used in the program this is done by using a worst case approach where the losses are calculated for the maximum junction temperature. The points for each area and current combination are compensated with this temperature factor, resulting in a slight increase in switching energy losses for the whole map. The temperature dependency varies for each area leading to a different temperature compensation for each area.

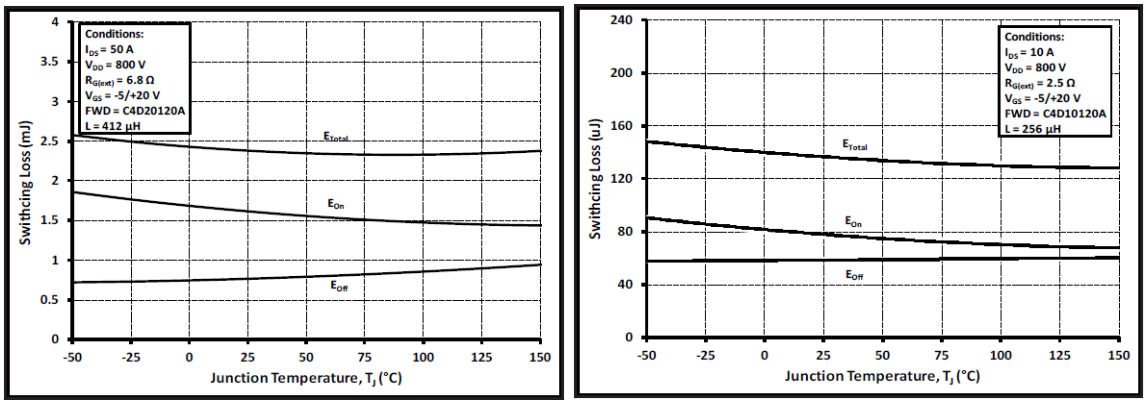

Fig. 18: Temperature dependency for the switching losses for Wolfspeed's discrete SiC MOSFET rated 25 Ω R_{ds} (left) and 160 Ω R_{ds} right), showing different temperature dependencies for different chip areas. Compensation for different gate resistances is also performed [24][40].

The switching losses also varies with the DC-link voltage. To be be able to adjust for the given DC-link voltage, the DTOP and V_{nom} is the voltage from the switching losses map given in the datasheets for each MOSFET size, in our case 800 V.

As seen in (35) k_v is a voltage compensation factor, which is calculated by comparing how the switching losses changes with different blocking voltage. It is calculated by evaluating k_v for each point in the E_{sw} curves in Fig. 17 above. This is done by fitting a third order polynomial to each of the switching losses curves and then solving for k_v for each current along the x-axis, thus getting the k_v needed to compensate for the difference between the curves. The equations for k_v (42) and (43) are shown in Appendix A.

The voltage factor k_v is calculated for all available SiC MOSFET datasheets, and then a weighted average is used for the final compensation factor. According to other studies of the value k_v is often approximated to 1.4 [5] for Si devices and the study made in this thesis gives a slightly lower value at 1.36 for SiC devices. The value is weighted for larger chip areas, since this is more frequently used in this study.

If the converter is run with the internal body diode instead of an external diode, the reverse recovery loss needs to be added to the switching losses. In this case they are not negligible as for the case with external diode [41]. Reverse recovery losses are calculated for the internal diode (3) and the MOSFET (4). The losses associated with reverse recovery is added to the switching energy losses according to (5) and thus increasing the total switching losses.

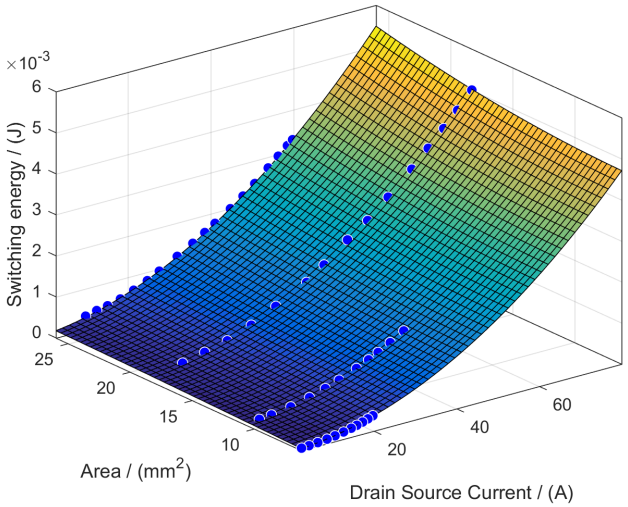

Fig. 19: Map used to estimate switching losses with temperature and area dependency, temperature dependency is created for each map and in this case compensated for 150° C.

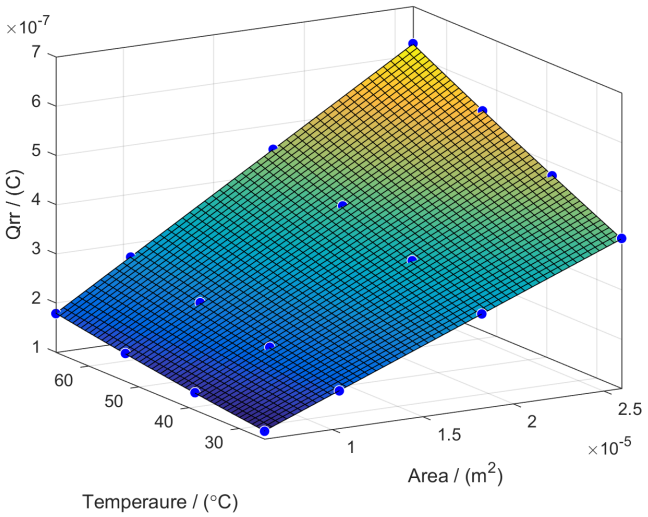

Fig. 20: Surface for estimating the reverse recovery losses added due to the use of the internal diode.

If the body diode is used for freewheeling the switching losses are given by (5). This uses the same switching energy map as the normal switching losses but adds the losses resulting from reverse recovery seen in Fig. 20. The Q_{rr} losses are temperature dependent as can be seen in (36). The temperature dependency of the reverse recovery losses are missing from the datasheets but can be significant for high temperatures [42]. This temperature dependency was taken from separate sources [42] [43].

$$Q_{rr} = 0.005T_j^2 + 1.7T_j + 120 \tag{36}$$

The temperature dependency is normalized around 25 $^\circ C$ and combined with the area dependency to create the map in Fig. 20.
In the MRC case there would be reverse recovery losses if the MOSFET was used in reverse conduction exclusively, but the diode is conducting in parallel and thus during blanking time, the voltage is forced to $V_d + R_d I_o$ during the transient resulting in no reverse recovery losses [33].

The accuracy of the switching energy map is very good and only deviates notably from the datasheet values at a few points. The coefficient of determination, CoD, for this map is 0.9999. It can be concluded that all of them are for very low currents for each respective area which is far from the normal operating point of each of MOSFET. Even though the deviations are large, the majority of the interpolated data points are within one $\%$ of the datasheet data point values.

B. Conduction losses MOSFET

The conduction losses of the MOSFET is calculated according to (6).The drain source resistance, R_{ds}, of the MOSFET varies depending on the area and temperature of the device giving the loss formula

$$P_{cond,M} = R_{ds}(A,T) I_{M,rms}^2 \tag{37}$$

Depending on how the freewheeling of the converter is performed, the conduction losses for the MOSFET are different. The simpler case, from a loss perspective, is if external Schottky diodes are used exclusively. In this case the total conduction losses for the MOSFET is given by 6. The current is here given from the DTOP and the drain source resistance, R_{ds}, is derived from datasheets. As can be seen in Fig. 21 on the right, the drain source resistance depends on the junction temperature of the chip. Within the operating area of the MOSFET shown in Fig. 21 below to the left, the I-V curve is considered linear and therefore R_{ds} is independent of current and voltage combination for each area. In this case the operating range is up to approximately 40 A, which is the rated current at 25° C.

Using the above functions and mapping them for each available bare die MOSFET area results in a area dependency for the R_{ds}. This is combined with the temperature dependency for each MOSFET resulting in Fig. 22. The map is used to estimate the $R_{ds}(A,T)$ for the MOSFET losses in general but also the currents for the MRC case since the resistance of the MOSFET is a factor that decides the current split.

The map for the drain source resistance of the diode can be seen in Fig. 22. The smallest area data points were omitted, since the behavior was very different for those, and in the main application for this optimization the component areas are significantly larger. With the final fit a CoD of 0.9998 was reached. A similar approach was used when modeling the forward resistance of the MOSFET body diode. Although the data was more limited with four different areas and three available temperatures for each area resulting in twelve I-V curves to extract data from in total. Since the conduction losses of the body diode results in a temperature increase of the MOSFET, this acts as a extra limiting factor. This means that a the size of the MOSFET needs to be increased compared to a similar case using external diodes. In figure Fig. 23 the I-V curves for the body diode can be seen. The resistance, R_f, is calculated as the inclination of the curve on the linear part marked as a red line on the figure to the right, and the threshold voltage V_{BD} is

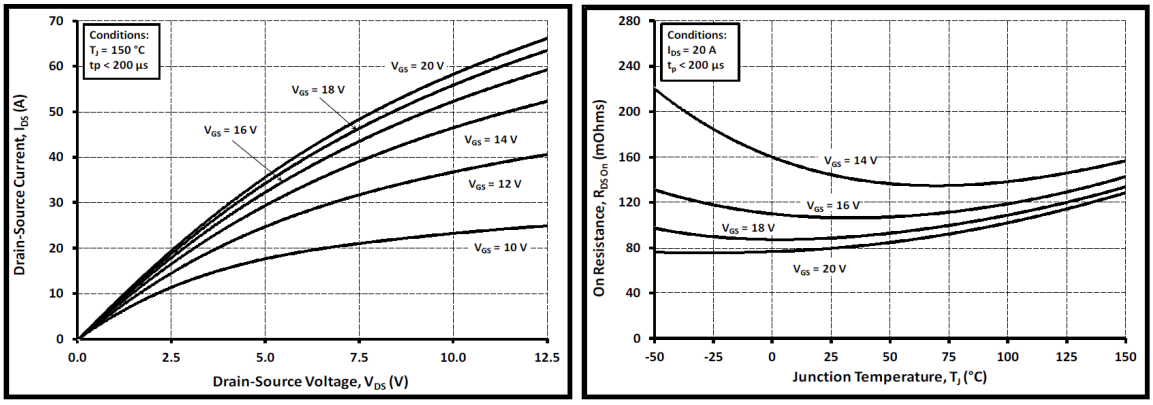

Fig. 21: V-I curve used to estimate R_{ds} for MOSFET rated for $80m\Omega$ (left) and Junction temperature and R_{ds} relation for the same component (right)[44].

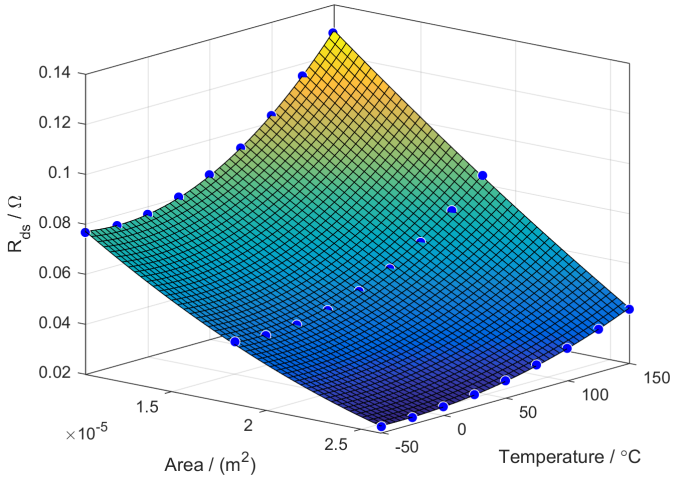

Fig. 22: By using datasheets for different size MOSFET's and mapping the area and temperature, a map was created to be able to estimate the R_{ds} for different combinations of those parameters for the optimization.

calculated where this line crosses the x-axis. These plots are for different bare die areas of the MOSFET but for the same temperature.

After extracting the data from from the graphs in Fig. 23 the data points where fitted to functions in MATLAB to be able to calculate the R_f and V_{BD} for each combination of area and temperature. Each of these resulted in the plots shown in Fig. 24 where the the linear part is first degree fit to the linear part of the function as shown by the line in the right figure of Fig. 23. Assuming the linear curve form $y = kx + m$ extracting the "k" value of the line gives the resistance of the body diode, R_f and the "m" value corresponds to the threshold voltage, V_{BD}. After this a map was able to be made for R_f and V_{BD} respectively, using the values gained from the I-V curves like in Fig. 24 for all areas and temperatures. The final results can be seen in figure Fig. 25 and Fig. 26. As can be noted in the map for the threshold

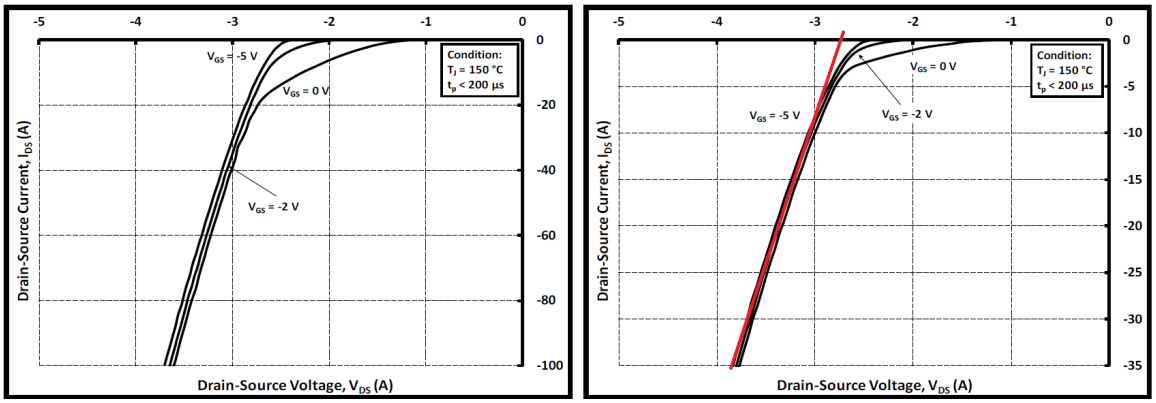

Fig. 23: V-I curve used to estimate R_f for the body diode of the MOSFET rated for $25m\Omega$ (left) and $160m\Omega$ (right) [24].

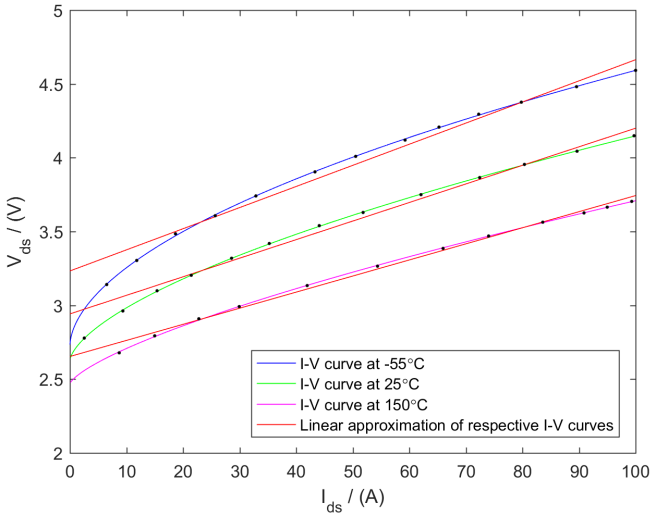

Fig. 24: I-V curves for the body diode of Wolfspeed's MOSFET rated 25 Ω, C2M0025120D. Note that the axes are inverted compared to normal I-V curves due to this making it easier to extract needed values from the plots.

voltage the the values for the lowest area was ignored for the fit due to strong deviation from the other values, this is further discussed in the discussion section of the thesis.

For the MRC case the conduction losses are modeled the same as in the other cases according to (6) and the resistances and threshold voltages are the same as in the other cases as well. The difference here is that the resistances also effect the current of the other component, e.g. the MOSFET resistance effects the diode current and vice versa as seen in (29) and (30). The map used to calculate this is seen in Fig. 22.

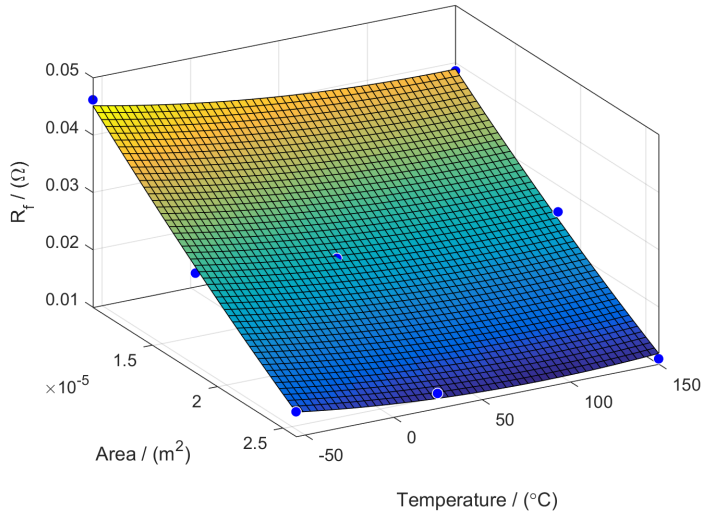

Fig. 25: Using the values for R_f that are derived according to text above a map was created and fitted to a polynomial surface that best fitted the data points.

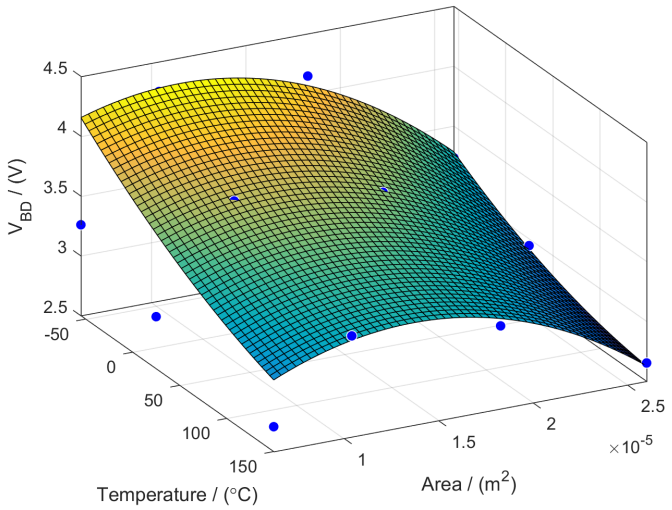

Fig. 26: The model of the threshold voltage of the body diode. Note that the data from the smallest MOSFET was exluded from this model, and the surface in the picture are not considering these data points.

The limited amount of data available proved to be a problem when trying to model the parameters of the body diode. As in most cases where the relation seemed to lack polynomial relations splines was originally used, but also using splines resulted in problems with connecting the data in reasonable ways. Finally the data points for the smallest area was ignored since they seemed to deviate to much from the pattern, strengthening the assumption made for the R_{ds} previously.

The surface in Fig. 25 have a CoD of 0.9953. Looking at the function for modeling the threshold voltage of the diode this one is also deviating from the data points to a certain extent even if smallest area data points are ignored, those data points are left in Fig. 26 to visualize how they deviate from the pattern. The CoD is 0.9928.

C. Conduction losses Diode

The diode losses are modeled in a very similar way as the conduction losses for the body diode that is explained in the previous segment. The losses were estimated using seven different bare die datasheets to be able to get a area dependency for the parameters. The parameters that need to be modeled for the diode losses are the forward resistance R_d and the threshold voltage for the diode V_d seen in (8). The modeling of the losses is made using (8) in both the MRC and MFD case, the difference being how the currents are modeled as can be seen in the theory chapter. The forward resistance for the diode had to be modeled slightly different then the R_{ds} of the MOSFET since no direct resistance data was available for extraction from the datasheets. Instead the data from I-V curves for each diode was gathered for five given temperatures per area as can be seen in Fig. 27. In the same way as for the body diode the linear part of the I-V curve was used for approximating the parameters and a first degree polynomial was fitted to the linear part of the curve. The result of this can be seen in Fig. 28.

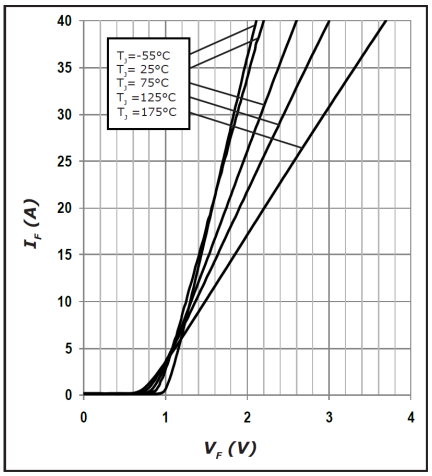

Fig. 27: This is the SiC Shottky diode I-V curves for the component C4D20120A from Wolfspeed. This is one out of seven available such I-V curves for different areas used to map threshold voltage V_d and forward resistance R_d [41].

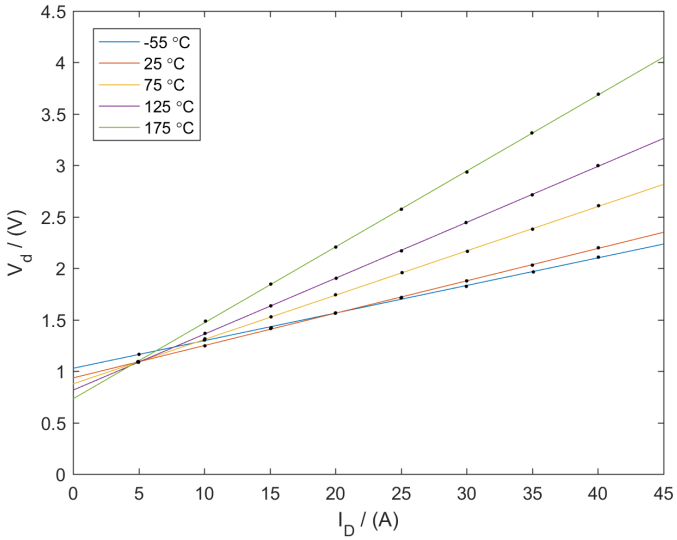

Fig. 28: Using the MATLAB program grabit, data points from the above datasheet was gathered resulting in several graphs like this one. These graphs is used to extract data needed to calculate the conduction losses of the diode and also the currents if reverse conduction is utilized. As in the case with the body diode the axes are inverted for practical reasons.

The results from these graphs were then combined and used to create a map for the R_d of the diodes depending on the area of the bare die and the junction temperature of the device. By comparing the two graphs it can be noted that they are mirrored, this is because of simple analytical reasons since it made it easier to extract the needed values. The resulting map for the R_d can be seen in figure Fig. 29. The Fit used here is a manual function fit created by using the fitting tool available in recent versions of MATLAB. This is used since no polynomials seemed to follow the surface in a way that fitted the more critical values in a good way. By using this tool a surface which was more correct for higher temperatures and areas was made.

The resulting surface shows a small temperature dependency where the forward resistance increases slightly for higher temperatures, but more importantly the resistance has a strong area dependency for all temperatures.

Finally the threshold voltage of the diode is calculated by looking where the lines in the function on Fig. 28 is crossing $I_D = 0$. The general behavior was the same for all bare die areas of the diodes, higher temperatures gives lower threshold voltages and lower temperatures gives higher threshold voltages. And as can be seen in Fig. 30 below, the area dependency of the threshold voltage is very small and is mainly due to temperature. In the same figure it can be seen clusters of data points for some certain temperatures and this is the data points of the same temperatures for different areas. As explained later in the discussion part, the area dependency is considered too small to have a real impact on the end result and was therefore ignored in the model. Instead an average of the forward resistances of the different bare die areas are chosen where the result is the linear interpolation in Fig. 30.

The diode forward resistance proved to be the hardest to fit to the data points and no polynomial or spline

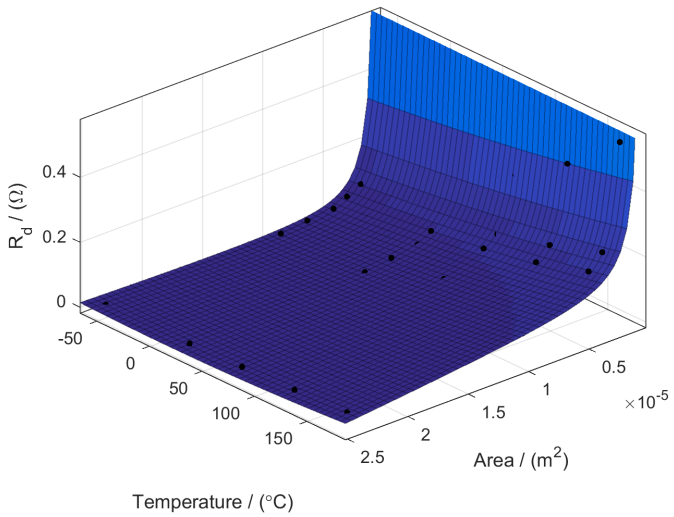

Fig. 29: Using the inclination of the functions for different temperatures as seen in Fig. 28 above the R_d for each combination of area and temperature is calculated and put into a map that is interpolated using a manual function.

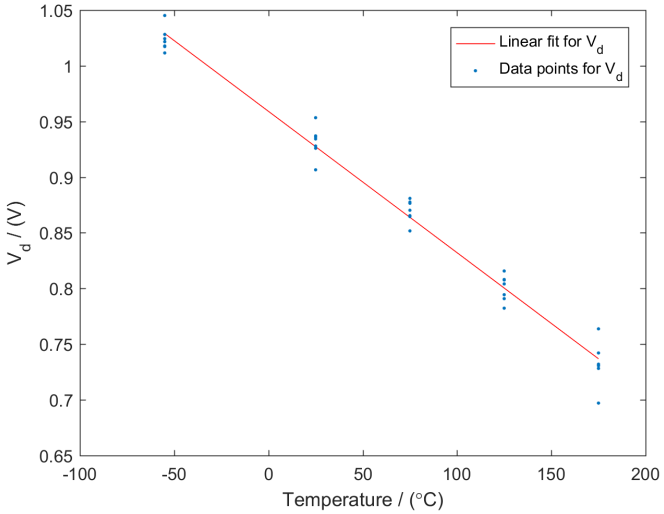

Fig. 30: Threshold voltage V_d for the external body diode with a temperature dependency. The blue dots for the same temperature represents different areas.

could do it in a way that the most important data points got a reasonable surface fit. For this purpose the fit in Fig. 29 is reasonably good with a deviation of 10.82 $\%$ this is also in the region where the fit is hardest to get perfect since the actual values of the R_d is very low relative to the maximum R_d which is for lower areas. These are as can be seen up to 75.99 $\%$ which makes this model very unreliable for small areas.

A result of this is that a new surface with the accuracy of the surface spread over more areas may need to be made for the reverse conduction case where the area of the diode is more variable. The threshold voltage of the diode Fig. 30 is more straightforward to model and the area dependency is totally left out of the model, as it only effected the model with a small margin. The CoD of this function is 0.9825.

D. Thermal network

The data provided in the datasheets for the discrete SiC MOSFETs is not sufficient to build a thermal model. Rth_{JC} is given, however the stack geometry is different in a power module, and both the TIM and the heat sink needs to be accounted for. From a FEM model of the thermal stack Fig. 31, including the TIM and the heat sink, an area dependent Rth_{JA} was simulated.

TABLE IV: Thermal model input parameters

Layer	Thickness [mm^2]	conductivity [W/(m K)]
SiC chip	-	125.6
Silver Sinter	0.1	100
Copper top	0.3	390
Si3N4 Ceramic	0.32	80
Copper botton	0.3	390
Silver Sinter	0.1	100
Copper Base plate	3	390
TIM	0.1	1
Aluminium Heat sink	0.4	300

The thickness of the block representing the heat sink is calculated from a given thermal resistance value, the area and the thermal conductance for a specific heat sink design with specified cooling conditions. The thickness is chosen so that the Rth_{SA} matches the value for the specific design. (State cooling conditions and Rth value) The resulting area dependent function for thermal resistance is shown in Fig. 32. The chosen ceramic for the model is a silicon nitride, which could be replaced by aluminum oxide or aluminum nitride which are the main ceramics in use [45]. Si3N4 was chosen however due to its low thermal resistance and large strength [46].

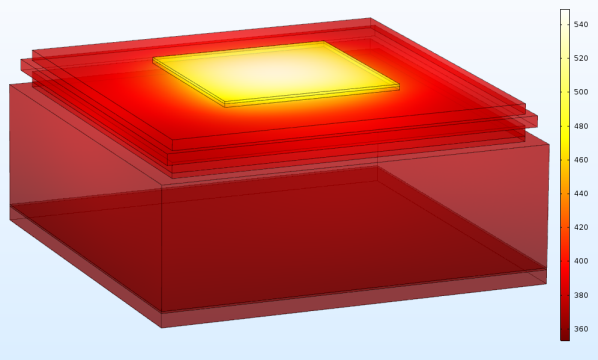

Fig. 31: Screenshot from the FEM simulation of the stack for the chip. The material and thickness of each layer is found in IV.

For the final thermal model it was decided that a constant chip to thermal area was to be used. In Fig. 33 k is a factor that shows how many times longer the side length of the thermal stack is compared to the semiconductor chip side length. The value for k was chosen to be 2.4 as a trade off where the thermal characteristics doesn't change very much if k is increased but a lower k value can drastically decrease the thermal capabilities of the chip. Fig. 32 is the function for the thermal resistance for $k = 2.4$ in Fig. 33.

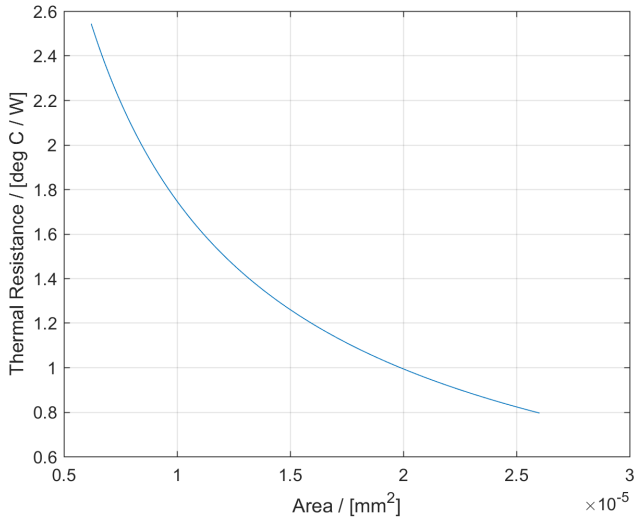

Fig. 32: The area dependent thermal resistance Rth_{JA} is shown here for the range of semiconductor chip area in this model.

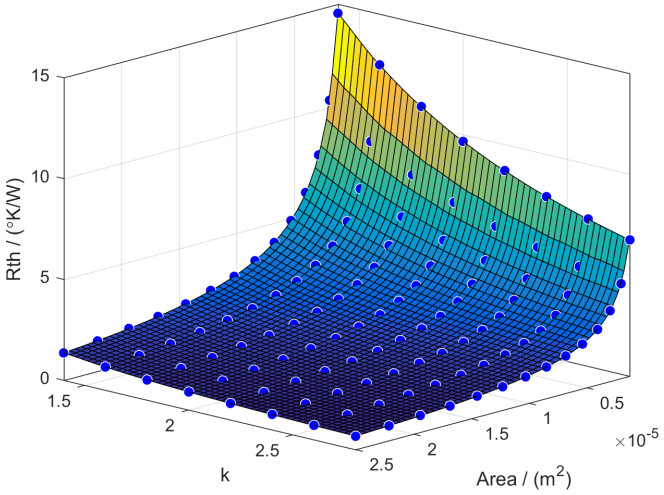

Fig. 33: This figure shows how the thermal resistance of the stack changes if the size of the stack relative to the chip area changes. k here is a factor that shows how many times larger the side length of the stack is in comparison to the chip.

E. Inputs

As mentioned there are a number of different inputs needed to make the optimization work. The majority of them comes from the DTOP but a few needs to be specified for this optimization specifically. Below is a list with needed inputs and their origin

a) From DTOP:

Phase current, I_{rms}
Switching frequency, f_{sw}
DC link voltage, V_{DC}
Modulation index, M
Power factor, PF or $cos(\phi)$

b) From User:

Ambient temperature (temperature of cooling medium), T_a
Maximum allowed junction temperature for MOSFET, $T_{j,max,M}$
Maximum allowed junction temperature for diode, $T_{j,max,D}$
Extra needed converter area or fill factor
Semiconductor cost per area for MOSFET and diode

c) From User, alternative:

Function for specific thermal characteristics in form of a junction to ambient thermal resistance function.

F. Currents

The phase currents to the motor can be divided into MOSFET- and diode currents. These currents are shown in the theory section and the final expressions are available in the appendix. The current combination used in this optimization is not necessarily optimized to fit a real case but are adjusted for a worst case scenario, with the maximum current through the MOSFET and the diode at the same time. This is needed to make sure the components can withstand the highest possible currents for each case without failing.

As explained earlier there are several alternatives for choosing the diodes. If comparing the case where the internal body diode is used to the external Schottky diode case, they are both experiencing the same amount of current seen in (23). This means that the current is calculated using the same formula for both cases, but the temperatures are still calculated according to how the loss-models differ for the two cases. For the internal case, the diode current adds to the losses of the MOSFET, thus increasing the temperature and in turn the area of the MOSFET further. For the external case, the diode current only affects the power losses and area of the Schottky diode. As explained in the theory chapter the case with reverse conduction differ, since the time period where each semiconductor conducts is a relation between the two components.

When identical parallel semiconductor units are connected together, the current splits evenly between the new components, and the total resistance is according to (39). Looking at only the relation between area and resistance for semiconductor devices, it always makes sense to connect fewer larger devices than a greater number of smaller devices. Since the application in this thesis is generally handling currents larger than the maximum for a single device this relationship can be utilized when optimizing the maps and functions needed to calculate the losses. Looking at Fig. 34 it can be seen that if the current exceeds the limit for a single component, the area for the two parallel devices are at least 50 $\%$. The currents used in the automotive industry are usually a few hundred amperes, which implies that several components are needed in parallel to be able to cope with the currents. This in turn implies that the optimization loop is working with areas at above 75- to 80 $\%$ at least, of the maximum area available from datasheets, even

when working with parallel components. Because of this the maps created for for example R_{ds} or E_{sw} are optimized for accuracy at larger areas and suffer from a slightly lower accuracy for lower areas. Another thing to consider when more devices are connected in parallel is that the the area between components, also becomes larger and further increases the size of the total converter and thus also the total cost of the converter. Finally it can be noted that the data in this thesis is restricted to a few bare die devices with limited area. And looking at newer devices this trend seems to continue and larger devices with better performance are soon on the market.

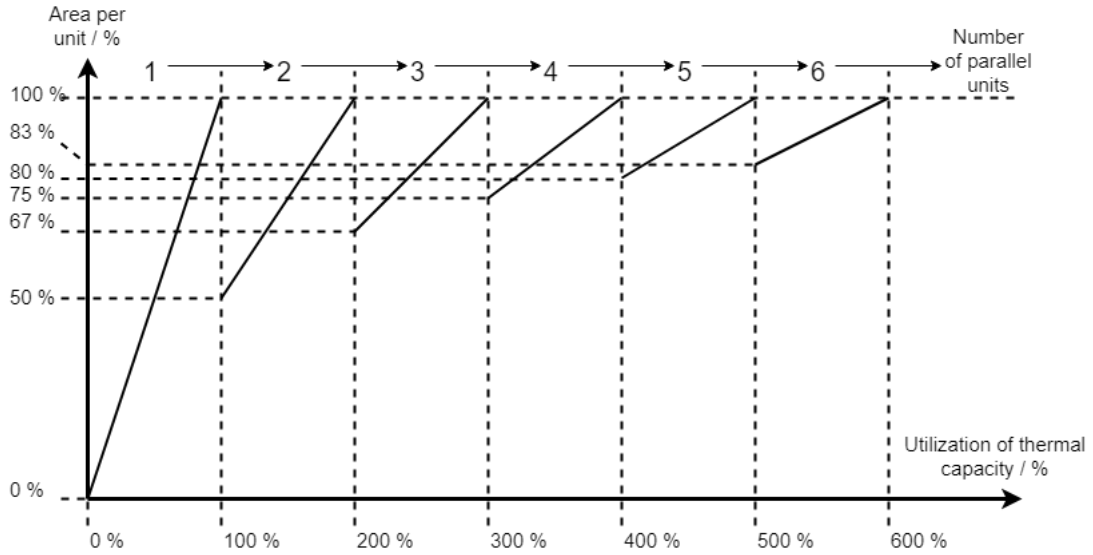

Fig. 34: The utilization of thermal capacity per silicon die for parallel connected components. The stated percentages on the y-axis are not exact, and the figure only represents the behavior of the parallel connecting of components. For example three components at exactly 100 $\%$ area won't correspond exactly to four components at 75 $\%$ due to non linearities in loss and thermal model.

G. Area optimization

The final goal of the optimization model is to optimize the total semiconductor cost of the converter and still meet the requirements of the input parameters. Throughout the optimization, area is considered the cost driver of the converter and therefore the semiconductors are optimized for minimum area. Two different modulation schemes, with and without reverse conduction, are implemented and they require different optimization approaches. The first optimization structure, without reverse conduction, can be seen in the flowchart in Fig. 35. In the flowchart there are a few key parts of the optimization

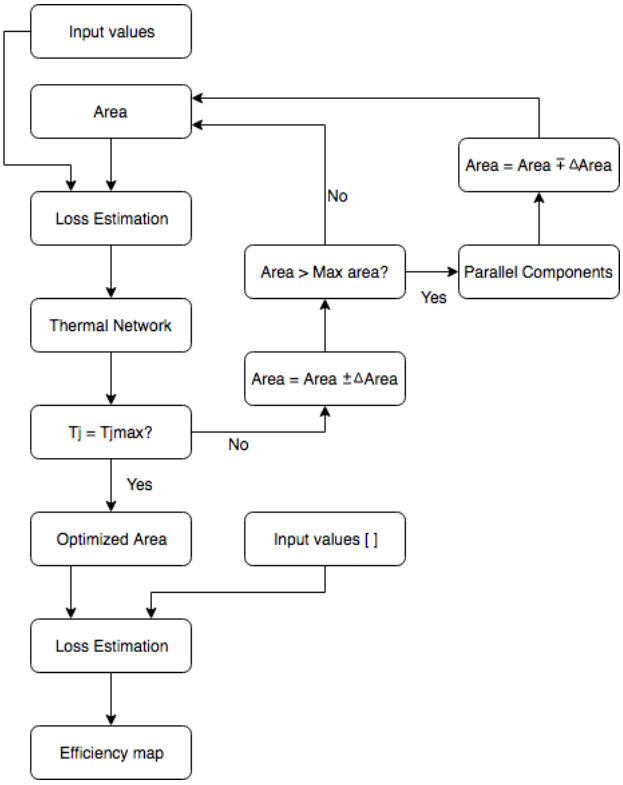

Fig. 35: Workflow of the area optimization program. Input parameters from the DTOP together with an initial area estimation allows for a primary loss estimation. From the calculated loss, an increase in junction temperature can be calculated with the thermal network. The new junction temperature is compared to T_{Jmax}, if it is too high, the area is increased to allow for greater power losses. If it is lower, the area is decreased to increase the junction temperature, as to utilize the full capability of the chip. If the chip area reaches its maximum value and the junction temperature is still too high, a parallel chip is added, the area adjusted, and a new loss estimation performed. With the optimized area as output, together with matrices of input values, an efficiency map for this area can be calculated.

that needs to be considered carefully to make sure the model is viable. These are the inputs, the loss estimation and the thermal network. The loss estimation can also be divided into switching losses and conduction losses, both for the MOSFETs and potential parallel Schottky diodes. The input values to the ”Loss Estimation” block in figure Fig. 35 are generated from a combination of the DTOP and data from datasheets for different SiC devices. This is further explained as each input is explained later in this chapter.

There are several alternatives how to implement the freewheeling current in a MOSFET converter. The alternative used for this version of the optimization is to use freewheeling diodes only. This is implemented in this thesis using SiC Schottky diodes in parallel with the MOSFETs and using a modulation scheme where the reverse conduction of the MOSFET is not utilized. A second alternative is to use a diode in parallel with the MOSFET but also use the MOSFET in reverse conduction mode, resulting in a current split between the MOSFET and diode. The third alternative is to use the parasitic body diode of the MOSFET as a freewheeling diode while not using the MOSFET in reverse conduction, this was not implemented due to the low performance of the body diode. The last alternative presented here is to only use the reverse conduction capabilities of the MOSFET, but this also means that the internal body diode is active during the blanking time. These different modes all have advantages and disadvantages, however this thesis have focused on the first two alternatives and the implementation of these are explained more thoroughly.

Looking at figure Fig. 35 the loop can be explained as follows. The first guess of chip area is used as a base in combination with the datasheet data to calculate the total losses of the semiconductor devices. After this the losses can be translated via the thermal calculations to a junction temperature for the chip of the given area. This is then compared to see if this area gives a junction temperature equal or close to the maximum allowed junction temperature. If this is not true the area is adjusted depending on if the temperature was higher or lower than the allowed. If the temperature was too high the area is incremented and if too low the opposite. This is then repeated until the junction temperature matches the maximum allowed temperature. The semiconductor devices in the model are limited to their respective maximum area, since they are based on real component data. This means that there is a possibility that the losses generated in each component, is too large for a single device to handle and thus the maximum allowed area for a single device is too small. If this is the case the program instead moves to the ”Parallel Components” block in figure Fig. 35, this means that more semiconductor devices are connected in parallel to be able to cope with bigger losses.

When the area is optimized to fit the maximum allowed temperature the optimization is done. This area is then used as a base in the DTOP and tested with a range of new inputs to get an efficiency map. This efficiency map is then used further in the DTOP to give a picture of the overall performance of the converter for a range of operating points. Finally to get the total area of the converter the area of the total amount of semiconductor devices are added together. This is also multiplied with a fill factor to take the thermal stack size and other external things into consideration in relation with the area. The fill factor is estimated to approximately 6, this means that the total converter area is 6 times larger than the semiconductor area. The fill factor can also be adjusted by the user if other dimensions are preferred.

Depending on which converter design is chosen, the starting parameters are made slightly different. For the case when only the diode is used for freewheeling, the initial guess for area is made close to the maximum for a single device. This is to make the convergence of number of parallel semiconductor components fast. As explained earlier, in most cases the current used for these applications is large enough so that more than one semiconductor device in parallel is needed. Every time the maximum area is reached for each number of parallel devices, a new device is added in parallel. If the total area for this number of parallel devices is still too small, a guess of an area close to the maximum is made for the next component. This makes the optimization connect an additional device in parallel without wasting iteration steps on trying different areas for too few parallel devices. This way of iterating can be seen in figure Fig. 34 and the iteration quickly gets to the right amount of parallel devices. This guess makes the iteration process fast if the number of parallel components is more than one.

TABLE V: Input parameters for area optimization.

Input	
Phase Current, I_{rms}	250 A
Maximum allowed junction temperature, $T_{j,max}$	125 $^{\circ}C$
Switching frequency, f_{sw}	10 kHz
DC-link voltage, V_{DC}	600 V
Ambient temperature	65 $^{\circ}C$
Modulation index, M	1
Power factor	0.9

1) Example of area optimization: Using the inputs shown in Table V and plotting the optimization loop per iteration for the MOSFET gives the results in Fig. 36. In the left figure is the area of MOSFET and in the right figure is the temperature. Looking at the temperature it can be seen that it reaches very high levels at the start but it quickly decreases to a level close to the wanted temperature which is $T_{j,max}$ in Table V. This quick convergence is due to the program adding more and more MOSFETs in parallel which splits the current between the components and therefore quickly decreases the temperature of the chip. If looking closely at the area figure it can be seen that the area is kept constant at this stage since the area is not adjusted, just the amount of parallel components. After five iterations the MOSFET is capable of handling the currents without causing a too high temperature and after this the area of the chips starts to change, in this case decrease slightly until the goal temperature is reached. At this point the minimal total area is reached. The same is also done with the diode and the figures are very similar.

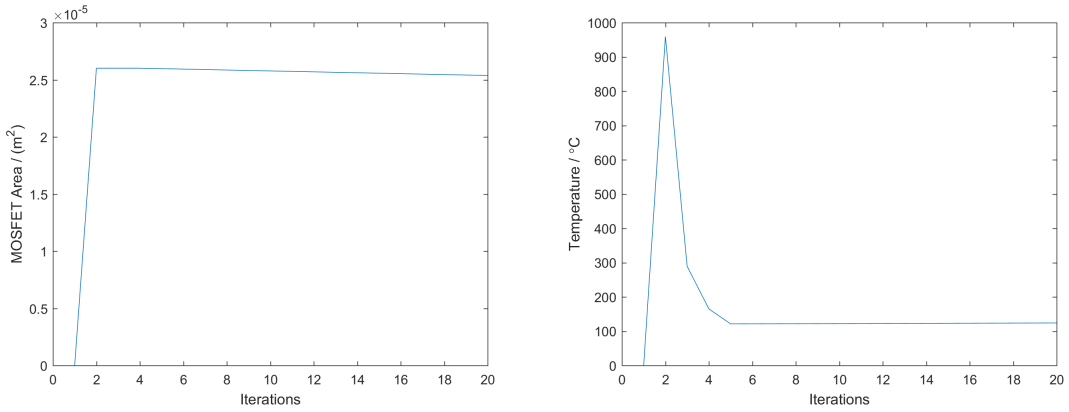

Fig. 36: To the left is the convergence of the MOSFET area if the input parameters in Table V is used, to the right is the corresponding temperature.

H. Cost Optimization, Reverse Conduction

If the MRC case is used, the paralleling becomes more sensitive and the amount of parallel semiconductor devices of one type affects the resistance relationship between the other semiconductor devices. For example if more MOSFET's are connected in parallel this lowers the total R_{ds} for that leg according to (39) and assuming that the diode didn't parallel simultaneously this makes more current take the freewheeling path through the MOSFET instead of the diode. This effect is illustrated in figure Fig. 37 and Fig. 38, note that this only illustrates effect of paralleling the resistances and does not take into consideration the threshold voltage of the diode. The formula for adding parallel resistances is given by

$$\frac{1}{R_{tot}} = \sum_{k=1}^{n} \frac{1}{R_n} \tag{38}$$

When all of the resistances added in parallel are the same size, meaning R_{ds1} is equal to R_{ds2} in figure Fig. 38 the total resistance R_{tot} is given by

$$R_{tot} = \frac{R}{n} \tag{39}$$

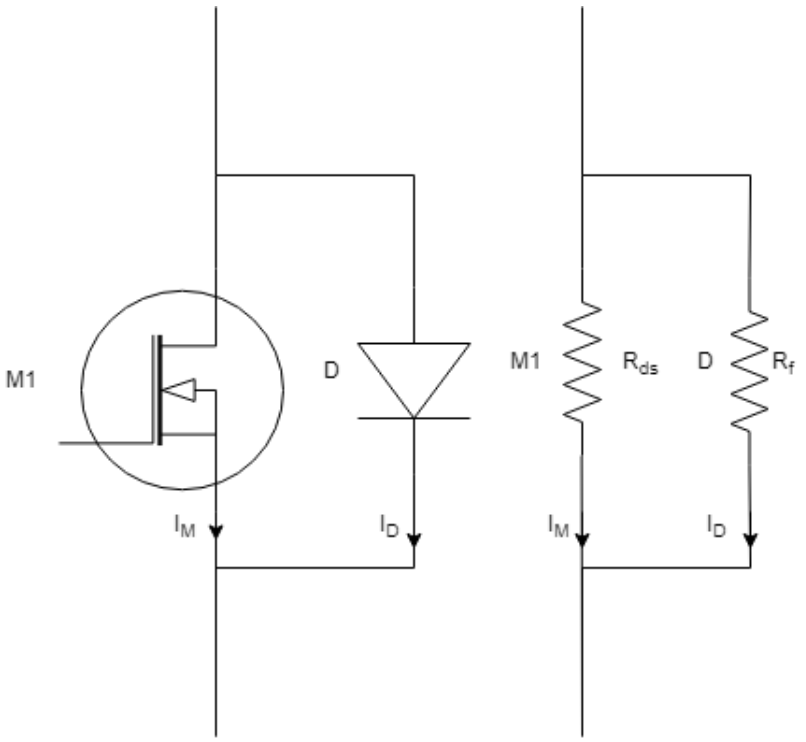

Fig. 37: A MOSFET in parallel with a diode (left) and the equivalent resistances during conduction (right). Note that the circuit does not model the threshold voltage of the diode.

This behavior makes a optimization loop as in the MFD case unreliable since the paralleling of a device greatly effects the development of the other. Therefore another solution was decided on for the MRC where the principle is shown in Fig. 39.

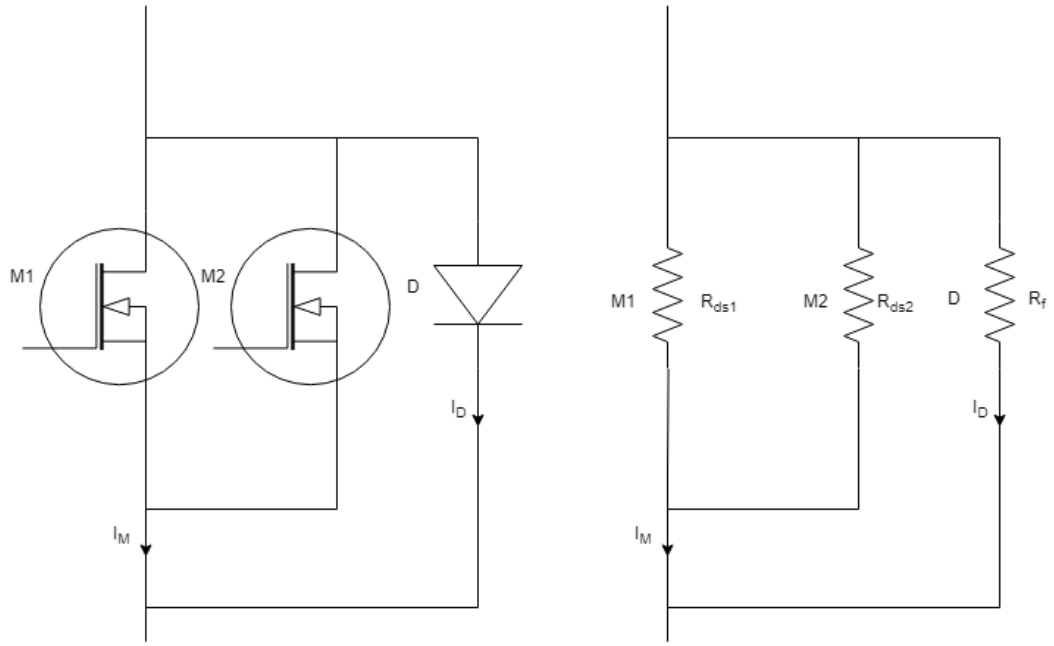

Fig. 38: In this case the inputs are at a level so that the converter is forced to add another MOSFET in parallel to cope with tougher specifications. The total resistance of the MOSFET leg (right) is now given by (39), and this leads to a current shift where a larger part of the total leg current runs through the MOSFET's. Note that the circuit does not model the threshold voltage of the diode

Instead of iterating to find the minimal area a matrix of all areas and numbers of diodes was created with a fixed resolution. The losses for all area combinations are then calculated and then the thermal calculations are done. Using this all area combinations with a temperature higher than the maximum allowed can be taken out of the matrix leaving only viable options. Then using the formula (40) the total cost of the devices can be calculated. After this the matrix is searched for a minimum cost value which gives the final result of the optimization.

$$Cost_{tot} = A_M Cost_M N_M + A_D Cost_D N_D \tag{40}$$

In (40) A_M and A_D is the area for the MOSFET and diode respectively, $Cost_M$ and $Cost_D$ is the cost per unit area for the diode. N_M and N_D is the total number of each device.

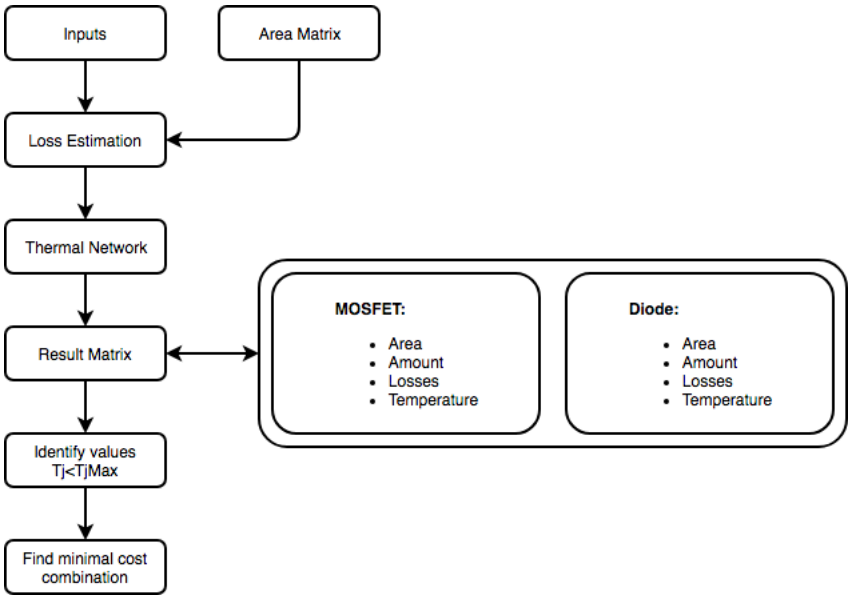

Fig. 39: Flowchart describing the flow of the cost optimization for the MRC case.

I. Model Accuracy and general limitations

To reduce complexity and increase usability, the model does not allow for altering the gate driver voltage. Both conduction and switching losses are dependent on the gate driver voltage, and the voltage used in the model is the maximum recommended operating gate source voltage of $-5\,V$ to $20\,V$.
The gate resistor value is also a fixed parameter in this program, to increase usability. All used data from the datasheets are specified with a gate resistor of $2.5\,\Omega$. The gate driver losses are not accounted for in this model with the motivation of them being negligible. With (41) one can calculate the power losses generated in the gate driver at a switching frequency f_{sw} and with supply voltage V_S when switching a MOSFET with the gate charge Q_G.

$$P_{GD} = V_S Q_G f_{sw} \tag{41}$$

J. Optimization efficiency

Since the main application of this loss model is to be integrated to the DTOP for a total vehicle optimization and therefore undergo up to millions of iterations, the speed of the optimization needs to be taken into consideration. This has been considered in a few ways. First the need to call separate scripts have been minimized this has been solved making the actual maps which in MATLAB are cfit objects into functions instead and putting those functions where they are used. This limits the usability of splined surfaces and this is one reason that the surfaces used in this thesis is based on polynomials or custom functions instead.

Another solution to increase the iteration speed is that all the maps are created on beforehand and not during the iterations. The drawback of this is that if the model is to be updated with data from new components this has to be done from scratch and then implemented in the model. Worth noting is that there is a big difference depending on what converter method is used. If the external diodes are used exclusively for the freewheeling currents the optimization for the diode and the MOSFET are separate from each other resulting in a total of 40-200 iterations.

V. Validation

In this section the validation process is presented. It proved difficult to acquire a physical power module, hence the presented validation process is of a non-practical nature. The circuit simulation tool LTSpice was used to validate the current split between MOSFETs and diodes.

A. Circuit simulation

A three phase converter model was designed in LTspice Fig. 40. LTspice is a simulation program for electronic circuits that lets the user record and analyze the behavior of a circuit. The voltage in all nodes and the current through any component can be analyzed in a waveform viewer. Power losses and other equations can be performed and plotted directly in the waveform viewer as well.

Synchronous three phase behavior is achieved with ideal switches and ideal diodes. The MOSFETs and diodes in each phase leg were replaced with component specific models of the MOSFETs and diodes from the Wolfspeed website [47], upon which the loss model was based. The ideal converter model was therefore used for validation of the different current splits. The different current splits corresponds to altering the gate driver conditions. The two different tested modulation schemes corresponds to modulation with and without reverse conduction. The gate drivers can be seen as the arbitrary behavioral voltage sources B1 to B6 in Fig. 40. To be able to compare the current split, a test with similar input parameters had to be done in the LTspice and optimization model respectively. To get the currents from the LTspice model it was run with the fixed input parameters being DC voltage, modulation index, switching frequency and load parameters. The same input parameters used in LTspice were then used in the optimization program. Other inputs like, power factor and calculated currents for the different components were taken from the LTspice model and used in the optimization program as well. After this the resulting currents in both models could be compared.

The condition whether the gate driver voltage is high or low, is set referring to the PWM controller circuit in Fig. 41. $V2$ is the sinusoidal reference wave, and $V3$ is the triangle modulation wave. That means that SPWM with no zero sequence current was implemented (MRC). $V5$ and $V4$ are set to distinct high and low levels. The RC circuit that follows the comparator is in place to allow for a blanking time at the MOSFET gates, and the condition of the gate drivers is set on the voltage over the capacitor. The blanking time is achieved by setting the top gate driver in each phase leg, to turn on only if V(n009) Fig. 42 is above 14 V. The lower gate driver is set to turn on only if V(n009) is below -1 V. The blanking time then corresponds to the time it takes for the voltage over the capacitor to drop from 14 V to -1 V, or to rise from -1 V to 14 V. If the condition was set at the same voltage level for both the top and bottom gate driver, this would correspond to no blanking time. The two gate drivers of each phase leg has turn on conditions based on the condition whether the gate driver voltage is high or low, is set referring to the PWM controller circuit in Fig. 41. $V2$ is the sinusoidal reference wave, and $V3$ is the triangle modulation wave. That means that SPWM with no zero sequence current was implemented (MRC). $V5$ and $V4$ are set to distinct high and low levels. The RC circuit that follows the comparator is in place to allow for a blanking time at the MOSFET gates, and the condition of the gate drivers is set on the voltage over the capacitor. The blanking time is achieved by setting the top gate driver in each phase leg, to turn on only if V(n009) Fig. 42 is above 14 V. The lower gate driver is set to turn on only if V(n009) is below -1 V. The blanking time then corresponds to the time it takes for the voltage over the capacitor to drop from 14 V to -1 V, or to rise from -1 V to 14 V. If the condition was set at the same voltage level for both the top and bottom gate driver, this would correspond to no blanking time. This was in the end done for the ideal switches since blanking time is not implemented in the loss model. The two gate drivers of each phase leg has turn on conditions based on equivalent PWM controller circuits as in Fig. 41, where the sinusoidal reference voltage v(N003) Fig. 42, is phase shifted 120 deg $^\circ$ between each leg.

For the case with no reverse conduction a gate driver condition is added. The condition states that, when the total current of the phase leg is negative, the upper gate driver is off. For the lower gate driver the opposite is true. When the total current through the phase leg is positive, the lower gate driver is off. This results in that the freewheeling current only goes through the external diode, parallel to the MOSFET (MFD).

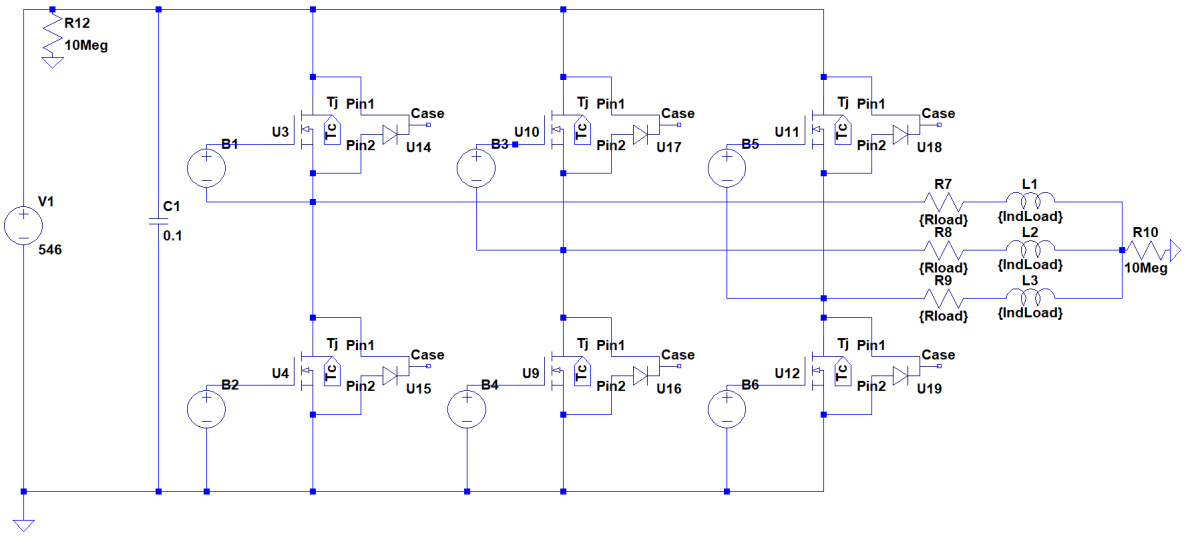

Fig. 40: The LTSpice three phase converter model used to validate the current splits in the loss model.

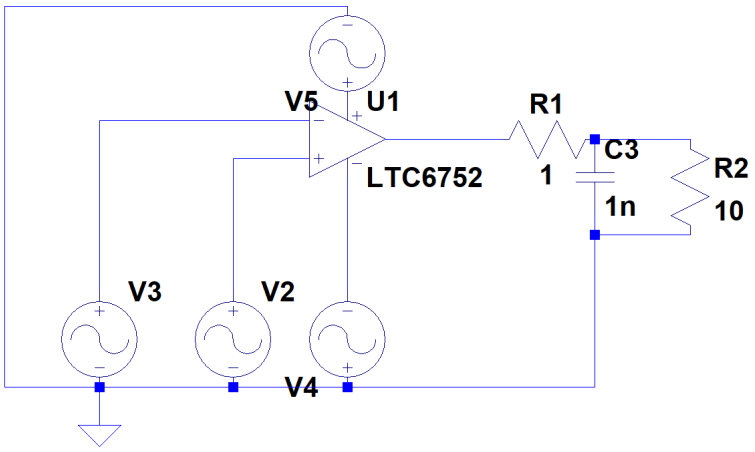

Fig. 41: The LTSpice PWM controller circuit, upon which the conditions for the gate drivers are based. $V2$ is the sinusoidal reference voltage, $V3$ is the triangle carrier wave and the condition of the gate drivers are set based on the voltage over the capacitor.

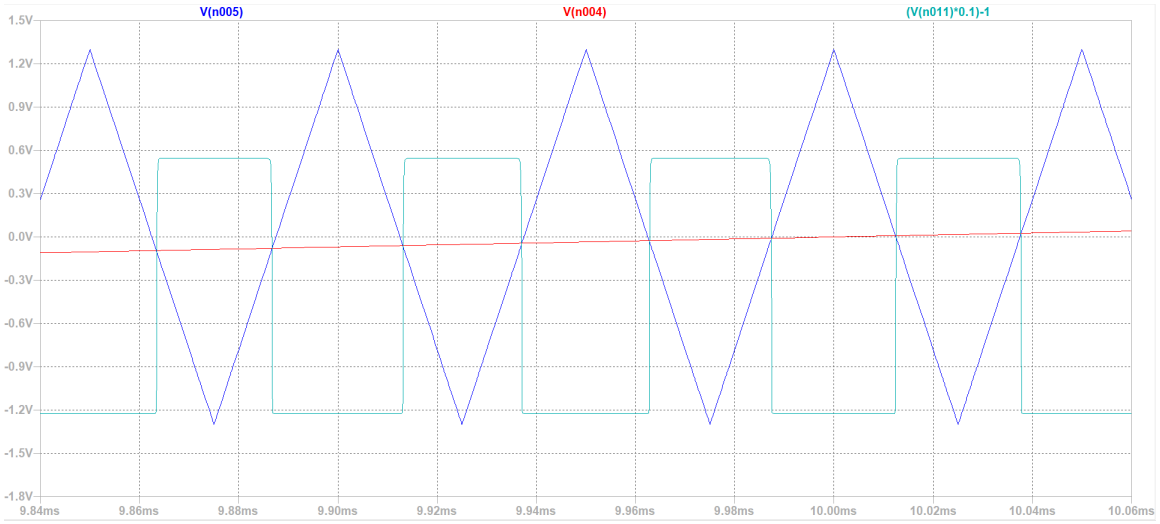

Fig. 42: The LTSpice gate driver voltages, generated in the LTspice gate driver circuit Fig. 41. The blue triangular wave is the carriewave, the red diagonal line is a section of the sinusoidal reference voltage. The cyan pulsed wave is the voltage over the capacitor and is what is used as reference for the output of the gate driver. Note that the voltage over the capacitor in Fig. 41 is divided by ten and has an offset of one volt to increase visibility.

B. Validation results

The results from the current split comparisons between the LTspice simulation and the loss model is presented in the tables below. The error is defined with the LTspice values as the reference, so that if the resulting current of the loss model is greater than the resulting current of the LTspice model, the error is positive.

TABLE VI: Simulation inputs run MFD 1

Unit	Magnitude	Unit
Peak phase current	26	A,
Modulation index	0.77	-
phase shift	0.104	rad.

TABLE VII: Simulation results run MFD 1

Unit	LTSpice	Loss Model	Error in %
MOSFET RMS current	11.64 A	11.81 A	1.46
Diode RMS current	5.62 A	5.44 A	-3.2
Total RMS current	18.40 A	18.38 A	-0.1

TABLE VIII: Simulation inputs run MFD 2

Unit	Magnitude	Unit
Peak phase current	36.77	A,
Modulation index	0.77	-
PF	0.063	-

TABLE IX: Simulation results run MFD 2

Unit	LTSpice	Loss Model	Error in %
MOSFET RMS current	16.69 A	16.71 A	0.1
Diode RMS current	7.69 A	7.67 A	-0.3
Total RMS current	26.09 A	26.00 A	-0.3

TABLE X: Simulation inputs run MRC 1

Unit	Magnitude	Unit
Peak phase current	36.77	A
Rds	0.07	Ohm
Ron	0.01	Ohm
Vd	0.8	V
nr of MOSFETs	1	-
nr of Diodes	1	-
Modulation index	0.385	-
PF	0.98	-

TABLE XI: Simulation results run MRC 1

Unit	LTSpice	Loss Model	Error in %
MOSFET RMS current	19.39 A	19.64 A	1.3
Diode RMS current	7.96 A	8.01 A	0.6
Total RMS current	32.52 A	32.53 A	0.03

TABLE XII: Simulation inputs run MRC 2

Unit	Magnitude	Unit
Peak phase current	36.77	A
Rds	0.06	Ohm
Ron	0.02	Ohm
Vd	0.8	V
nr of MOSFETs	1	-
nr of Diodes	1	-
Modulation index	0.385	-
PF	0.98	-

TABLE XIII: Simulation results run MRC 2

Unit	LTSpice	Loss Model	Error in %
MOSFET RMS current	19.95 A	20.12 A	0.9
Diode RMS current	6.37 A	6.40 A	0.5
Total RMS current	32.61 A	32.53 A	-0.3

TABLE XIV: Simulation inputs run MRC 3

Unit	Magnitude	Unit
Peak phase current	142	A
Rds	0.03	Ohm
Ron	0.03	Ohm
Vd	0.8	V
nr of MOSFETs	1	-
nr of Diodes	1	-
Modulation index	0.85	-
PF	0.98	-

TABLE XV: Simulation results run MRC 3

Unit	LTSpice	Loss Model	Error in %
MOSFET RMS current	68.15 A	67.90 A	-0.4
Diode RMS current	9.81 A	9.95 A	1.4
Total RMS current	101.48 A	100.41 A	-1.1

TABLE XVI: Simulation inputs run MRC 4

Unit	Magnitude	Unit
Peak phase current	53.2	A
Rds	0.03	Ohm
Ron	0.03	Ohm
Vd	0.8	V
nr of MOSFETs	1	-
nr of Diodes	1	-
Modulation index	0.85	-
PF	0.84	-

TABLE XVII: Simulation results run MRC 4

Unit	LTSpice	Loss Model	Error in %
MOSFET RMS current	25.58 A	25.79 A	0.8
Diode RMS current	2.19 A	2.27 A	3.7
Total RMS current	37.60 A	37.62 A	-0.1

Reviewing the resulting currents in the LTspice model and the corresponding currents for the optimization model in, it can be concluded that they differ very marginally compared to each other. This in turn implies that the analytical expressions used to model the components are good enough to be used in a pre-design phase of a full converter circuit.

VI. Results

In this section the various results of this thesis is presented. It will go through the outputs and behavior of the area optimization with the different modulation schemes. The results of a comparison between running the DTOP with a SiC MOSFET PEC or a Si IGBT PEC will also be presented.

A. Area Optimization Results

This section presents two typical sets of input parameters XVIII and XXI where all the input parameters available in the optimization program are shown. The DC voltage is the output voltage of the traction battery, switching frequency refers to the switching frequency of the three phase converter. Peak phase current, power factor and modulation index is discussed in the theory section. The ambient temperature is the temperature of the cooling medium in the thermal model. The maximum junction temperature is the highest temperature that the model allows a given semiconductor component to reach. The output tables for MRC XX, XXIII and MFD XIX, XXII presents the following; the number and area for each semiconductor component, the total semiconductor area, and the corresponding semiconductor cost. The typical behavior of the two modulation schemes are also presented in Fig. 43 and Fig. 44. The cost figures presented as results are presented in a fictive currency, $X\$$, where the cost for MOSFET dies and diode dies $Cost_M$ and $Cost_D$ in (40) was set to 1 $X\$/[mm^2]$ and 0.7 $X\$/[mm^2]$ respectively. It's worth noting the difference in number of diodes in the results of the two different modulation schemes, as well as the total area and cost.

TABLE XVIII: Parameter Specifications for run 1

Quantity	Magnitude	Unit
DC voltage	600	V
Switching frequency	20	kHz
Peak phase current	400	A
Power Factor	0.9	-
Modulation index	0.9	-
Ambient temperature	65	°C
Maximum junction temperature	125	°C

The optimization program run with the input parameters from XVIII produces the following two different sets of output, by running the two different applied modulation schemes. The results in XIX show that the number of diodes is not far from that of the MOSFETs and it can also be noted that the diodes have a considerable die area. The need for these diodes comes from that the diodes will carry the full free wheeling current since reverse conduction of the MOSFETs is not used in this modulation scheme.

TABLE XIX: Results of the area optimization, run 1 MFD

Quantity	Magnitude	Unit
Single MOSFET Area	23.1	mm^2
Single Diode Area	22.7	mm^2
nr of MOSFETs in parallel	5	-
nr of Diodes in parallel	4	-
Total semiconductor Area	1238	mm^2
Cost of semiconductor Area	1076	$X\$$

In XX, the results from the optimization program with reverse conduction enabled is presented. The main thing to pay attention to, is that the number and die size for the diodes have decreased significantly compared to XIX. The reason for this reduction is that the freewheeling current can now be carried by the MOSFETs. This result shows that enabling reverse conduction of the MOSFETs can reduce the total semiconductor die area by 38 $\%$. The reason for still having the diodes is to eliminate the reverse recovery

TABLE XX: Results of the area optimization, run 1 MRC

Quantity	Magnitude	Unit
Single MOSFET Area	25.0	mm^2
Single Diode Area	1.4	mm^2
nr of MOSFETs in parallel	5	-
nr of Diodes in parallel	1	-
Total semiconductor Area	760	mm^2
Cost of semiconductor Area	757	$X\$$

losses of the MOSFETs. It should be noted that the cost reduction (29 $\%$) is smaller than the reduction in semiconductor area. The reason is that the decrease in semiconductor area comes from a decrease in the cheaper diode dies whereas the more expensive MOSFET die area has actually increased. To explain the results in a more general sense, the output from the optimization program can be used as a starting point for sizing and designing a SiC MOSFET three phase converter.

In Fig. 43 the four main output variables, number of diodes, MOSFETs and the corresponding die size, are presented with only peak phase current varied. The number of each component and the component area can be seen to follow the same principals. When fewer components of greater size reaches the maximum available size, the are replaced by more smaller ones. When adding an additional component, the die size is only reduced so much that the total semiconductor area is still increased.

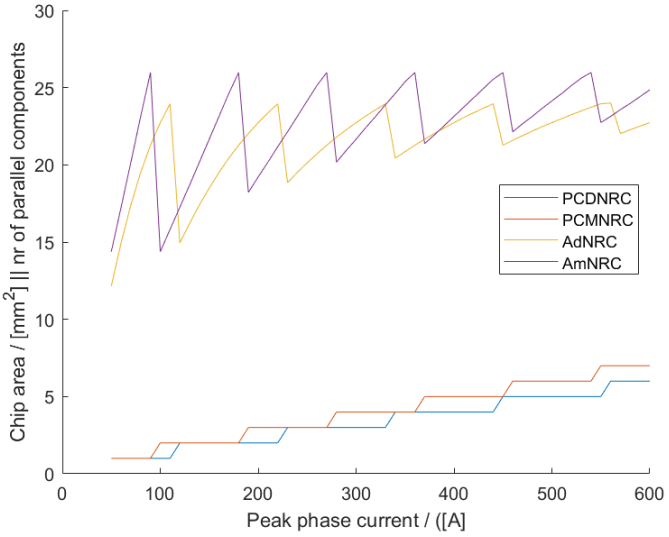

Fig. 43: The behavior of the MFD optimization. Blue: number of diodes in parallel. Red: number of MOSFETs in parallel. Yellow: Die area for the diode. Purple: Die area for the MOSFET. The number of MOSFETs increase with peak phase current. This is also seen for the diodes. The area of each components increases until the maximum component area has been reached, then an additional component is added in parallel.

In Fig. 44 the same four main output variables are presented. The similar behaviour of the two components is no longer present, however it can be seen that the behaviour of the MOSFETs resemble what was seen

in Fig. 43. The MOSFET behaves the same way since it still carries substantial currents. A swifter increase in area and number can be seen since the MOSFET also carries parts of the freewheeling current.

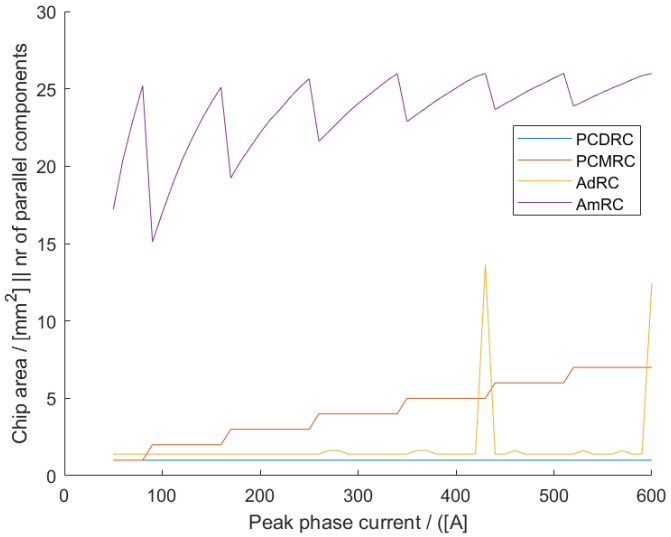

Fig. 44: The behavior of the MRC optimization. Blue: number of diodes in parallel. Red: number of MOSFETs in parallel. Yellow: Die area for the diode. Purple: Die area for the MOSFET. The number of MOSFETs increase with peak phase current, this is not seen for the diode. The area of the MOSFET increases until the maximum chip area has been reached, then an additional MOSFET is added in parallel. The diode does not increase in size since the main purpose of the diode is to eliminate the reverse recovery losses of the MOSFET, it doesn't really carry any large currents. The spikes seen in diode area is a resolution defect, increasing the resolution removes the spikes.

The following tables XXI, XXII and XXIII follow the same structure as the previous three tables. It shows the results from the two different modulation schemes, with a different set of input parameters.

TABLE XXI: Parameter Specifications for run 2

Quantity	Magnitude	Unit
DC voltage	600	V
Switching frequency	15	kHz
Peak phase current	550	A
Power Factor	0.9	-
Modulation index	0.5	-
Ambient temperature	65	°C
Maximum junction temperature	125	°C

Just as with the previous set of input parameters the number and size of the two semiconductor components correlate for MFD. The diode area is about 78 % of that of the MOSFET. The ratio between the two areas is affected by both the switching frequency and the modulation index.

TABLE XXII: Results of the area optimization, run 2 MFD

Quantity	Magnitude	Unit
Single MOSFET Area	23.9	mm^2
Single Diode Area	22.4	mm^2
nr of MOSFETs in parallel	6	-
nr of Diodes in parallel	5	-
Total semiconductor Area	1534	mm^2
Cost of semiconductor Area	1331	$X\$$

For MRC the same behavior can be seen as with the previous set of input parameters. The higher peak phase current has just barely increased the diode size whereas the MOSFET area has significantly increased. The diode has the effect of eliminating the reverse recovery losses of the MOSFET but other than that carries little current.

TABLE XXIII: Results of the area optimization, run 2 MRC

Quantity	Magnitude	Unit
Single MOSFET Area	24.5	mm^2
Single Diode Area	1.6	mm^2
nr of MOSFETs in parallel	7	-
nr of Diodes in parallel	1	-
Total semiconductor Area	1040	mm^2
Cost of semiconductor Area	1037	$X\$$

Comparing the two different modulation schemes it can be seen that MRC enables a reduction in semiconductor area. With a strong correlation between semiconductor area and cost it is interesting to compare the total chip cost of the two modulation schemes. In Fig. 45, this is shown for a range of peak phase currents. For the set of parameters used a 25 $\%$ reduction in total chip cost can be achieved by enabling MRC.

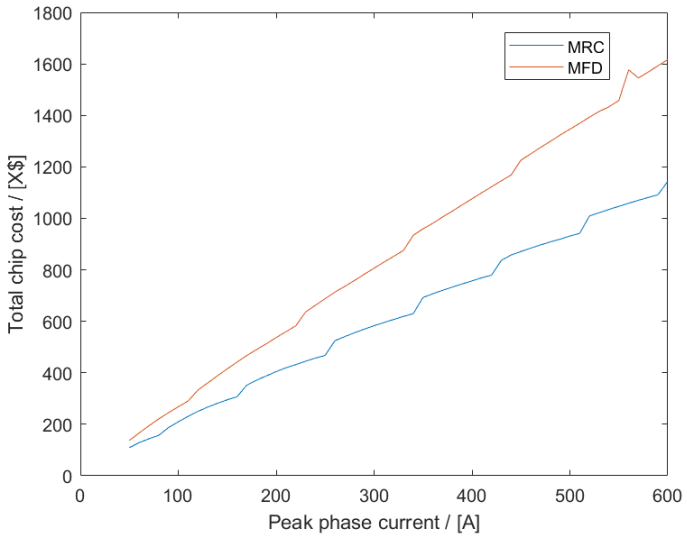

Fig. 45: System cost for MRC and MFD as a function of peak phase current. A 25 $\%$ cost reduction can be observed with the use of MRC.

To be able to get a view of how the optimization model affects a total power train design the SiC optimization model is implemented into the DTOP. This makes it possible to compare different power train designs, using different semiconductor technologies.

Fig. 46 visualizes this difference. Each dot in the figure is a different power train design that fulfills the predetermined demands. Around two thousand machines is tested for each semiconductor type and a single speed gearbox is used in the DTOP. The different attributes of the powertrain have been optimized to provide lowest possible objective function which in this case is cost. These attributes are for example the length of the particular electrical machine geometry, number of turns and the rated current of the converter.

Dots present to the right in Fig. 46 is more expensive power train designs. This means that the given electrical machine geometry is poorly suited for the application and some component in the drive train has to be oversized to be enable the drive train to meet the demands. The opposite can be said about dots to the left in the same figure.

Finally it should be noted that the objective function for this simulation is exclusively cost and not efficiency. If efficiency was to be introduced as an objective it can be expected that a higher cost could result in a higher efficiency. Comparing the different semiconductor technologies it can be seen that Si has the powertrain designs with the lowest costs but the SiC based power train designs generally has a higher efficiency.

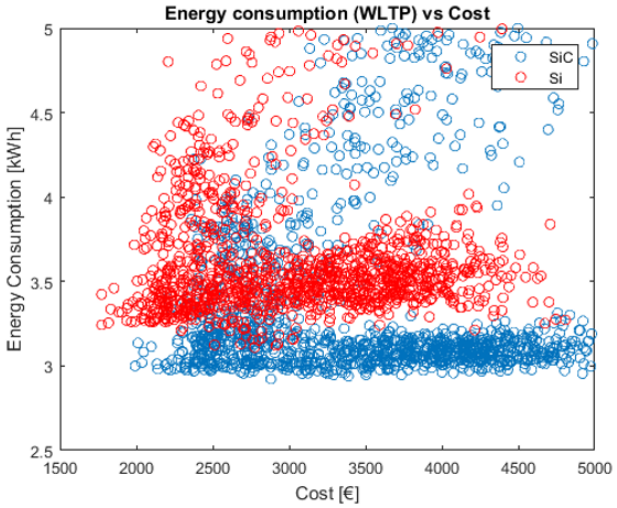

Fig. 46: Energy Consumption versus cost simulation of a complete electric vehicle (output from the DTOP). The input variables for the DTOP can be seen in Fig. 1. Each circle is a resulting drivetrain design that meets the performance requirements of the input. A trend of the system using SiC being more efficient is present. Regarding the cost, it can be seen that it is generally lower for the system using Si.

VII. Discussion

Approximations made and decisions taken during the design of the optimization program are motivated and a discussion about the results of the program is presented. The validation process is evaluated along with the overall limitations of the model.

A. Optimization model design

The drain source resistance of the MOSFET has a current dependency. It's negligible for the major part of the operating region, but for larger currents the dependency becomes more apparent. The current dependency is not implemented in the model with the motivation that running a component with such a high current would cause a too high junction temperature. However if the model is run with a very low ambient temperature and the cooling structure is more efficient, larger currents could be pushed through the component. Without the current dependency implemented, this causes an increasing error with increasing the current of the devices respect to the nominal current for its size. Designing the drain source resistance model, the data from the smallest MOSFET was removed. This was motivated by the visual inspection of the 3D surface that describes the function. The resistance of the smallest MOSFET was small enough to worsen the fit significantly for the larger areas. Since the main area of use for this model is for higher power-levels, the focus is to optimize for a more accurate fit for bigger MOSFETs.

The same procedure was followed with the same motivation for the function describing the threshold voltage of the body diode of the MOSFET. Furthermore the precision of the body diode threshold function was lowered by the lack of data points. The datasheets did simply not contain a consistent high number of data points, upon which to base a precise model. Since both the values for the R_{ds} and the R_f and V_{BD} are taken from the same datasheets it can be concluded that there is some fundamental difference between the smallest bare die MOSFET and the larger ones since those graphs deviated from the rest in all cases.

The model for switching losses is implemented with an area specific temperature dependency. As the program evolved the temperature dependency was rejected at the benefit of simply calculating the switching losses with a function depending on area and drain source current. When this was done the temperature was fixed to 150 °C. This could be done after a study was performed about how much the temperature actually influences the magnitude of the switching losses, as shown in XXIV. The error in the table is the maximum total error for each area, when comparing a temperature of 150 °C to 25 °C. With such a small maximum error, for such a large temperature change, the temperature dependency was removed.

TABLE XXIV: Switching loss temperature dependency

Area$/[mm^2]$	**Drain source current**$/[A]$	**Error**$/\%$
26	60	0.8
18	50	1.9
10	40	-4.8
6	20	-6.8

Without reverse conduction both the diode and the MOSFET are essential for the converter to function, so in this case, the different cost for diode and MOSFET doesn't change the optimization in terms of area or cost. In other words, optimizing for minimum area is the same as optimizing for minimum cost. This means that the optimization of the two components can be done completely separate, once for the MOSFET and once for the diode. For the case with reverse conduction it is not equivalent to optimize for minimum cost and to optimize for minimum area, since the area of the two components affect each

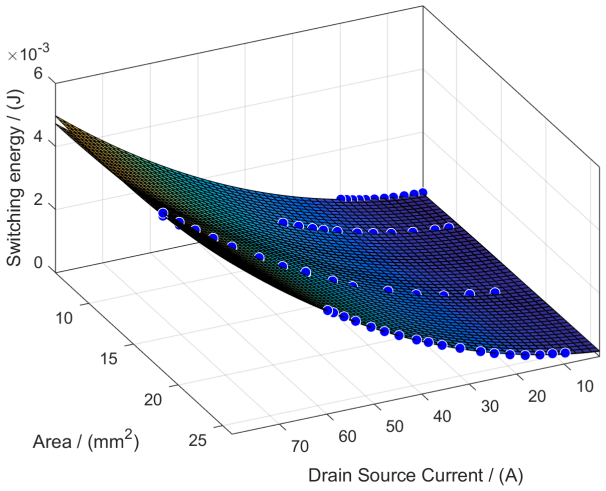

Fig. 47: Looking at the two maps there can only be seen a small difference, further implying that the temperature dependency for the switching losses are small.

other and changes the current split. This means that the conditions are altered during the time of the optimization. As explained earlier if the MOSFET reaches a point where a parallel connection is needed, this decreases the total resistance for the MOSFETs and therefore as an effect of this, decrease the current through the diode. This is what motivated the two different optimization approaches.

With a more in depth analysis of the thermal characteristics of parallel connecting devices, it is possible that several smaller semiconductor components may be more beneficial than fewer larger ones. With the thermal model used in this thesis fewer larger semiconductor components is however the optimal solution. The reason for this is that the thermal model does not incorporate the effects of each semiconductor component being heated by nearby semiconductor components.

Not a lot of effort has been put into matching gate driver circuits with the MOSFETs. The gate capacitance of the MOSFET increases with larger die sizes, which puts greater demands on the gate drivers.

In the theory section higher operating temperature of SiC is mentioned, however the loss model in this thesis was based on SiC MOSFETs with a specified maximum junction temperature of 150 degrees [24], which is also common for power Si IGBTs in datasheets [48]. This means that the benefit of the general higher temperature capability of SiC components, is not seen in any of the results.

In this loss model, transient thermal fluctuations were not calculated and instead a safe margin was set to the maximum allowed junction temperature. This margin can be decreased or increased depending on expected operation scheme. The temperature margin might for example need to be increased if the converter is expected to handle operating points with low fundamental frequencies and high currents for longer periods of time. This could correspond to a heavy vehicle starting in a hill.

B. Result discussion

The single small diode along with several big MOSFETs that is a common result of the optmization with MRC, is a topic of discussion. Indeed the current through the diode can be very small, especially with several big MOSFETs in parallel. With available parameters, this is the least costly solution however blanking time is not accounted for in this model. During blanking time the current must be carried through the parallel diode. With the diode only being sized for the small currents carried by the diode during parallel conduction, the full amplitude blanking time currents may result in too much power losses for the diode even though they are short pulses.

It can be tempting to think that saving additional semiconductor area by removing the diode completely is beneficial. This is however wrong, since removing the diode introduces the reverse recovery losses of the body diode which are substantial. Fig. 48 shows the additional losses added if the parallel diode is removed completely. For higher currents it is clear that the diode in parallel is beneficial for the system.

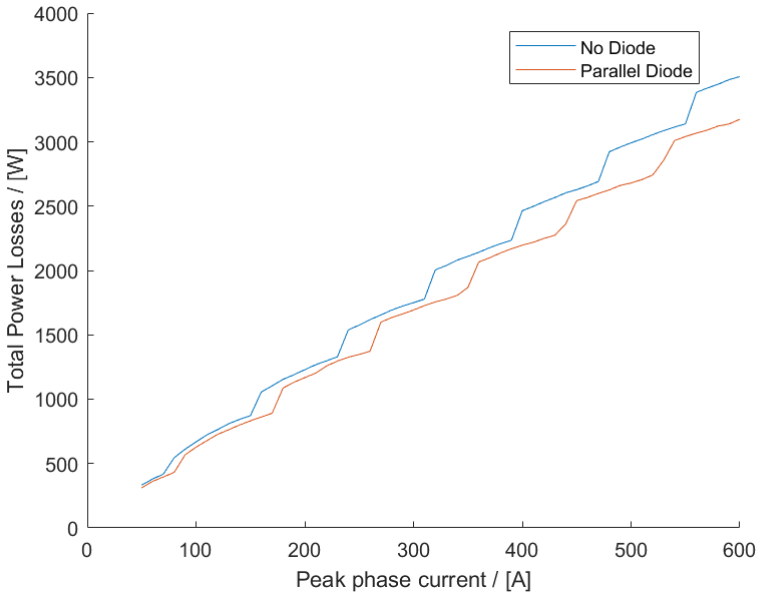

Fig. 48: The additional power losses from removing the parallel diode is shown. Blue shows the power losses without parallel diode, red shows the losses with a parallel diode.

The implementation of blanking time would also influence the sizing of components in MFD. The change in sizing would probably not change as much as for MRC, since the diodes are already sized to handle the full amplitude blanking time currents, because the amplitude is the same as during free wheeling. If MFD and MRC are influenced differently by blanking time, one should be careful with what conclusions are drawn from this model, taking no account for blanking time.

C. Drivetrain optimization

One effect from switching to silicon carbide MOSFETs from silicon IGBTs, is that the switching rise time is shorter. This causes more high frequency components to be present in the system, which can cause more losses and wear in the motor [3]. With the current design of the DTOP this is not considered, and should be recognized by the user.

In the theory section higher potential switching frequencies of SiC is mentioned. In real applications this would lower the ripple on the output current. The improved current would in turn lower the losses of the electric machine. This effect is however not be seen in this optimization since the DTOP doesn't consider the current ripple to the motor.

With the seniority of the IGBT technology and the SiC MOSFETs being such a young technology, one should be careful as to which conclusions is drawn from the comparison between the two. The SiC devices are developing quickly and even the ones used for this thesis are outperformed by newer versions. Most likely the SiCs will continue to improve rapidly in terms of performance whilst the performance improvements on IGBTs is more stagnant.

The loss model is in its entirety based on datasheets of discrete components, but it aims to model a power module where SiC bare dies would be used in reality. The reason for this is simply that the model was on what little data that was available. Comparing the datasheets of the bare dies and the discrete components, many times the graphs are exactly the same but sometimes the graphs differ slightly. Another motivation for choosing to model the converter based on the discrete components is that the bare die datasheet lack data on the switching behavior and losses. In the early stages of the project there was an intent to use the thermal data from the datasheets as well. This idea was later rejected since the thermal characteristics differ significantly between discrete components and power modules.

Many of the component models were difficult to fit well to the gathered data points, a solution to this could be using splines. Splines were however avoided in the development of this optimization program for a few reasons. The first being that it is impossible to operate a splined surface outside of the limits defined by the data points. This may cause unnecessary crashes when for example the resulting temperature is too high. Another reason to avoid splines is to decrease the iteration time of the optimization. Splines can not be made into equations in MATLAB and therefore the map needs to be loaded which costs extra time. Therefore there had to be a trade off between using the splines which usually had a better overall precision for the surface, or to use polynomial fits / custom equation fits which where faster and also did not result in a crash even if a value was calculated outside of the gathered data points. The problems was mostly overcome by using polynomials and custom equations that is better fitted to the more common operation points of the optimization program. This means that higher temperatures and areas were prioritized over the opposite.

VIII. Conclusion

The area optimization program outputs results that match the obvious hypothesis; that higher currents results in larger and more semiconductor components. Changing single input parameters helped validate a correct behavior of the model, however an in depth validation of the magnitudes of the losses was never performed. Without reverse conduction the need for both MOSFETs and diodes is obvious. When optimizing for area with reverse conduction, the model behaved according to the hypothesis that adding diodes is not area efficient, why the model ultimately removed the diodes.

There has been related work to this report, with area optimization of semiconductor components. The real contribution of this thesis is the in depth modeling of losses of SiC MOSFETs. It is a step towards realizing and embracing the potential of SiC MOSFETs in many different applications.

A lot of time was spent reaching out to manufacturers of SiC components, to get datasheet upon which we could base our model. None were accommodating to our needs, and the model was thus based on the datasheet of the one manufacturer that were willing to share their bare die sizes of their SiC components. During some time, efforts were made to acquire cost data for SiC semiconductor components and for gate driver circuits, again no contacts proved helpful and the process was rendered time consuming with few results.

With only a few weeks left until the project deadline, the necessity of modeling reverse conduction in MOSFET converters was discovered. It had been encountered earlier in the project but was along with supervisors dismissed as an uncommon feature. During the final weeks of the thesis a lot of time was put into correctly modeling the current split during reverse conduction. Enabling reverse conduction however led to the option of eliminating the diode completely, which would demand additional modeling of the reverse recovery losses of the MOSFET. This additional modeling was never performed due to time constraints. In addition it was no longer a viable option to just optimize for smallest area, since the cost for SiC diodes is smaller than the cost of SiC MOSFETs. A revision of the optimization method was made to accommodate for the fact that the size of each component directly affects the current split and so the size of the other component. The initial time plan for the project we believe was sound, however it is difficult to predict the mistakes and issues that come with a large scale project as this.

A. *Future Work*

A Validation process for the losses in the area optimization should be seen as the next step of this work. The currents in the model are validated and the theory of the loss models is well established and widely used. However, for the model to be validated as reliable, it should be compared to a finished power module and its power losses. This could either be done in a lab environment with a real module. A substantial upgrade to the loss model would be to implement blanking time. The current split should be revalidated with blanking time, and a more accurate relation between MFD and MRC could be presented.

New cooling topologies are being developed, such as integrated pin fin for power modules. This means that the heat sink is integrated into the base plate of the power module, instead of using an external where the Achilles' heel is the TIM. Developing and integrating a loss model for such a topology and others, would make the model more versatile.

As SiC MOSFETs gets more well established in the market, and the technology matures, cost will probably decrease as performance increases. This means that this loss model will be outdated, but simply an update of component characteristics and cost data would render it useful again. As bare die data becomes more available with time, the loss model could be expanded to include switches and diodes from several different producers.

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APPENDIX

A

$$E_{sw/600V}(I_{ds})(\frac{V}{V_{ref/600V}})^{k_v} = E_{sw/800V}(I_{ds})(\frac{V}{V_{ref/800V}})^{k_v} \tag{42}$$

Solving for k_v gives

$$k_v = \frac{\log \frac{E_{sw/800V}(I_{ds})}{E_{sw/600V}(I_{ds})}}{\log \frac{V}{V_{ref/600V}} - \log \frac{V}{V_{ref/800V}}} \tag{43}$$

APPENDIX

B

$$ImosfetRMS := \left(\frac{Io^2 M\cos(\phi)}{3} - \frac{Io^2 M\cos(\pi - \phi + \beta)}{8} + \frac{Io^2 M\cos(3\pi + \phi + 3\beta)}{24} - \frac{Io^2 M\cos(\pi + \phi + \beta)}{4} - \frac{Io^2 \sin(2\pi + 2\beta)}{8} + \frac{Io^2 \beta}{4} + \frac{Io^2 \pi}{4} - \frac{1}{48\pi (Rd + Ron)^2} \left(6\cos(-2\pi - \phi + \beta)\, Io^2 MRd^2 \right.\right.$$

$$+ 3\, Io^2 MRd^2 \cos(-2\pi + \phi + \beta) - Io^2 MRd^2 \cos(-6\pi - \phi + 3\beta) - 3\, Io^2 MRd^2 \cos(\pi - \phi + \beta) + Io^2 MRd^2 \cos(3\pi + \phi + 3\beta) - 6\cos(\pi + \phi + \beta)\, Io^2 MRd^2 + 24\, MRd\, Io\, Vd \cos(\phi)\, \beta - 12\, MRd\, Io\, Vd \cos(\phi)\, \pi$$

$$- 3\, Rd^2 Io^2 \sin(-4\pi + 2\beta) - 3\, Rd^2 Io^2 \sin(2\pi + 2\beta) + 12\, Rd^2 Io^2 \beta - 6\, Rd^2 Io^2 \pi - 6\, MRd\, Io\, Vd \sin(-4\pi - \phi + 2\beta) - 6\, MRd\, Io\, Vd \sin(2\pi + \phi + 2\beta) + 24\, Vd\, Rd\, Io \cos(-2\pi + \beta) - 24\, Vd\, Rd\, Io \cos(\pi + \beta)$$

$$\left. + 12\cos(-2\pi - \phi + \beta)\, MVd^2 - 12\cos(\pi + \phi + \beta)\, MVd^2 + 24\, Vd^2 \beta - 12\, Vd^2 \pi \right)$$

$$\left. + \frac{\frac{Io^2 M\cos(-2\pi - \phi + \beta)}{4} + \frac{Io^2 M\cos(-2\pi + \phi + \beta)}{8} - \frac{Io^2 M\cos(-6\pi - \phi + 3\beta)}{24} - \frac{Io^2 \sin(-4\pi + 2\beta)}{8} + \frac{Io^2 \beta}{4} - \frac{Io^2 M\cos(2\pi + \phi)}{4} - \frac{Io^2 M\cos(-2\pi + \phi)}{8} + \frac{Io^2 M\cos(6\pi + \phi)}{24} - \frac{Io^2 \sin(4\pi)}{8}}{2\pi} \right)^{1/2}$$

Fig. 49: Final MOSFET rms current expression

$$ImosfetRMS := \left(\frac{Io^2 M\cos(\phi)}{3} - \frac{Io^2 M\cos(\pi - \phi + \beta)}{8} + \frac{Io^2 M\cos(3\pi + \phi + 3\beta)}{24} - \frac{Io^2 M\cos(\pi + \phi + \beta)}{4} - \frac{Io^2 \sin(2\pi + 2\beta)}{8} + \frac{Io^2 \beta}{4} + \frac{Io^2 \pi}{4} - \frac{1}{48\pi (Rd + Ron)^2} \left(6\cos(-2\pi - \phi + \beta)\, Io^2 MRd^2 \right.\right.$$

$$+ 3\, Io^2 MRd^2 \cos(-2\pi + \phi + \beta) - Io^2 MRd^2 \cos(-6\pi - \phi + 3\beta) - 3\, Io^2 MRd^2 \cos(\pi - \phi + \beta) + Io^2 MRd^2 \cos(3\pi + \phi + 3\beta) - 6\cos(\pi + \phi + \beta)\, Io^2 MRd^2 + 24\, MRd\, Io\, Vd \cos(\phi)\, \beta - 12\, MRd\, Io\, Vd \cos(\phi)\, \pi$$

$$- 3\, Rd^2 Io^2 \sin(-4\pi + 2\beta) - 3\, Rd^2 Io^2 \sin(2\pi + 2\beta) + 12\, Rd^2 Io^2 \beta - 6\, Rd^2 Io^2 \pi - 6\, MRd\, Io\, Vd \sin(-4\pi - \phi + 2\beta) - 6\, MRd\, Io\, Vd \sin(2\pi + \phi + 2\beta) + 24\, Vd\, Rd\, Io \cos(-2\pi + \beta) - 24\, Vd\, Rd\, Io \cos(\pi + \beta)$$

$$\left. + 12\cos(-2\pi - \phi + \beta)\, MVd^2 - 12\cos(\pi + \phi + \beta)\, MVd^2 + 24\, Vd^2 \beta - 12\, Vd^2 \pi \right)$$

$$\left. + \frac{\frac{Io^2 M\cos(-2\pi - \phi + \beta)}{4} + \frac{Io^2 M\cos(-2\pi + \phi + \beta)}{8} - \frac{Io^2 M\cos(-6\pi - \phi + 3\beta)}{24} - \frac{Io^2 \sin(-4\pi + 2\beta)}{8} + \frac{Io^2 \beta}{4} - \frac{Io^2 M\cos(2\pi + \phi)}{4} - \frac{Io^2 M\cos(-2\pi + \phi)}{8} + \frac{Io^2 M\cos(6\pi + \phi)}{24} - \frac{Io^2 \sin(4\pi)}{8}}{2\pi} \right)^{1/2}$$

Fig. 50: Final diode rms current expression

$$IdiodeAVG := -\frac{1}{16\pi (Rd + Ron)} \left(-4\, Io\, MRon \cos(\phi)\, \beta + 2\, Io\, MRon \cos(\phi)\, \pi + Io\, MRon \sin(-4\pi - \phi + 2\beta) + Io\, MRon \sin(2\pi + \phi + 2\beta) - 4\, Ron\, Io \cos(-2\pi + \beta) + 4\, Ron\, Io \cos(\pi + \beta) - 4\, M\cos(-2\pi - \phi + \beta)\, Vd + 4\, M\cos(\pi + \phi + \beta)\, Vd - 8\, Vd\, \beta + 4\, Vd\, \pi \right)$$

Fig. 51: Final Diode avg current expression